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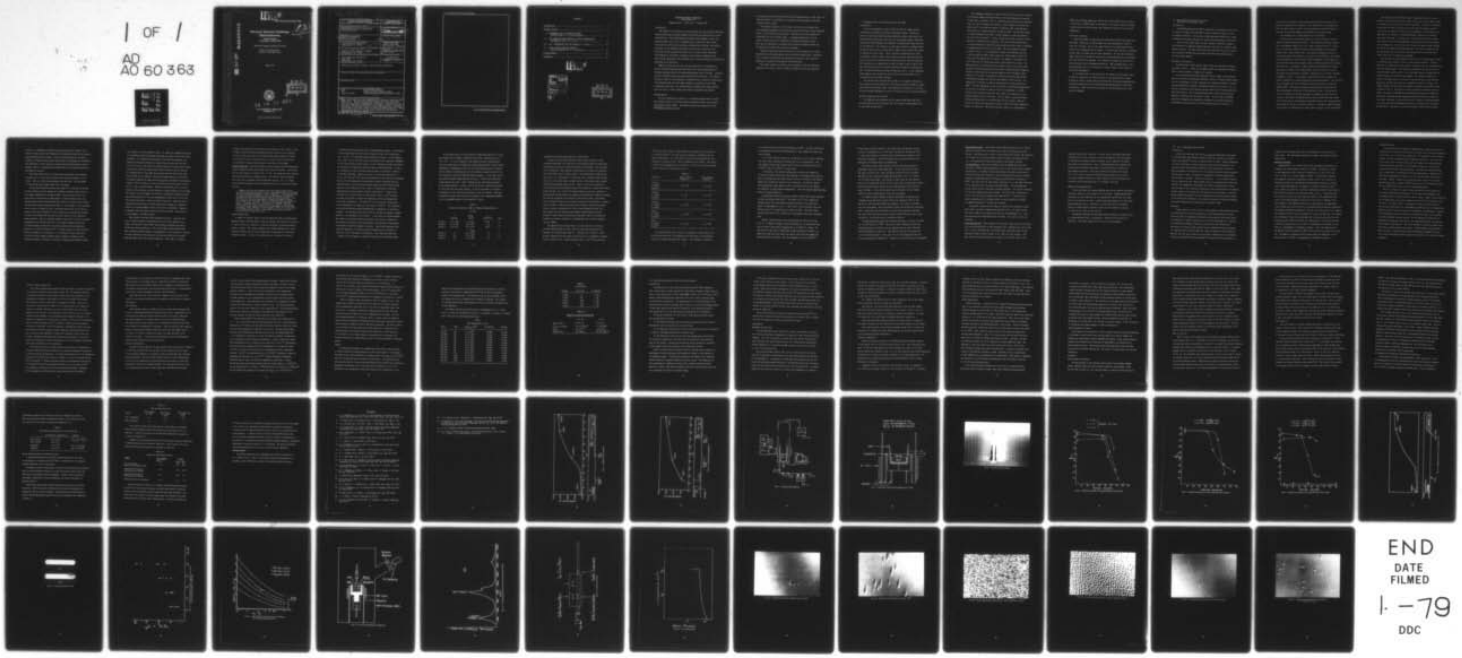

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NRL Memorandum Report 3845

Electronic Material Technology (Semiconductors)

Summary Report
1 July 1976 - 30 April 1978

Edward M. Swiggard and Howard H. Lessoff

Materials Technology Branch
Electronics Technology Division

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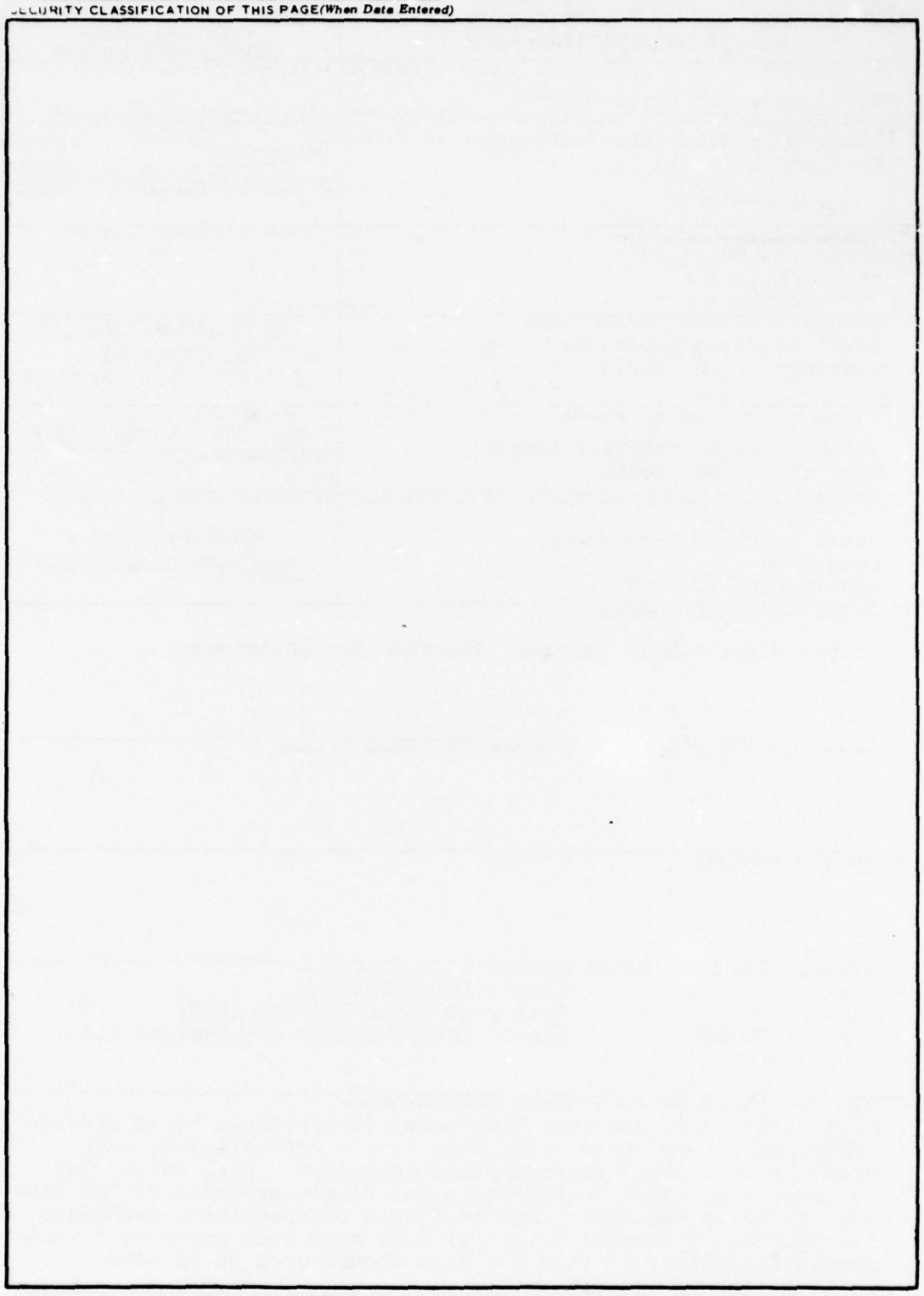

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ELECTRONIC MATERIAL TECHNOLOGY
(Semiconductors)

Summary Report - 1 July 1976 - 31 March 1978

Introduction

The advance of electronics into the microwave and the millimeter frequency regions have placed stringent demands on materials and especially the active semiconductors. Those semiconducting materials which appear to offer the greatest promise are the III-V compounds and in particular GaAs and InP. There have been and are many problems concerning the electronic and chemical properties of the compound semiconductors which must be solved so that electronic devices prepared from them will be a truly viable technology. This program was developed to determine those material parameters which affect device application and performance and to develop methods of reproducibly preparing useful materials.

Emphasis during the last year has been directed at a) improving the quality of semi-insulating GaAs substrates and b) determining methods of reducing trapping states at the substrate-epitaxial layer interface. Attention was also directed at preparing semi-insulating InP substrates. The results obtained to date in this program are coordinated with a materials characterization program at NRL such that rapid feedback is available at each stage of material processing. The characterization feedback helps define needed areas for work to further improve the material preparation and growth.

Program Outline

The III-V semiconductor effort is a coordinated program which involves the combined efforts of the Naval Research Laboratory (NRL), and the Naval Ocean Systems Center (NOSC). The material growth and preparation effort

Note: Manuscript submitted July 27, 1978.

is performed within the Electronic Material Technology Branch of NRL, while the characterization is performed by a coordinated effort managed by the Semiconductor Branch at NRL.

The material program is a broad based activity which considers that each processing parameter must be rigidly controlled from the initial elemental purity to the final device evaluation. Therefore the current program was subdivided into the following tasks: a) compound preparation; b) bulk single crystal growth and c) substrate finishing and epitaxial growth. Each step in processing is evaluated with continuous feedback between the characterization effort and the material program.

Samples of materials prepared were and are being submitted to various laboratories for characterization and use in device fabrication. Techniques used to prepare the material are continuously reported to the scientific community via technical presentations and publications.

This report presents the status of the program to date and additional information on specific areas is readily available from the investigators.

I. Compounding GaAs in Pyrolytic Boron Nitride (PBN)

Introduction

With the development of the GaAs FET the need for higher-quality reproducible substrates has become increasingly evident. Because the surface of most semi-insulating GaAs substrates becomes electrically conducting during the heating cycle prior to liquid phase epitaxy (LPE) many laboratories have abandoned this approach to preparing FET layers directly on the substrate. The situation in vapor phase epitaxy is somewhat better in that an in-situ etch is being used to remove a thin surface layer prior to growing the active layer. Even in VPE most laboratories have found it necessary to grow a buffer layer between the active layer and the substrate to prevent out diffusion of an unknown acceptor from the substrate. The situation in ion implantation is much the same as that in LPE in that less than 25 percent of the crystals tested are suitable for implantation due to surface "conversion" during the annealing cycle. A more fundamental understanding of the properties of GaAs will be required before we can successfully overcome these problems.

The approach that has been taken by NRL is to compound a high purity GaAs charge and use this material to grow single crystals of GaAs by liquid encapsulation Czochralski (LEC). This approach has allowed us to initiate selective doping experiments in order to access the role of various impurities.

Synthesis Apparatus and Procedure

The apparatus and procedures used to prepare high purity GaAs have been described in detail elsewhere[1] but for the sake of completeness will be described briefly again.

The predominant impurity in GaAs is silicon[2] and is a result of attack on the quartz ampoule by gallium vapor at the high temperatures required to melt GaAs. As shown in Fig. 1, a pyrolytic boron nitride boat and inner liner are used to minimize the reaction. Vacuum baking the gallium and arsenic prior to sealing the ampoule is important when using PBN boats since there is a slight wetting of the boat by GaAs. The wetting results in convex interfaces which have a strong tendency to trap gas bubbles at the solid liquid interface. A piece of high purity GaAs is placed in the seed well to minimize this occurrence. The seed allows solidification to proceed smoothly and prevents supercooling which often leads to formation of trapped gasses and voids in the ingot. The vacuum baking apparatus is shown in Fig. 2. It is important to adjust the temperature profile so that the gallium oxides (which deposit at 465°C) deposit beyond the point where the ampoule will be sealed. The ampoule is evacuated to 8 x 10^{-7} Torr and the gallium and arsenic vacuum baked for 16 hours. The baking furnace is rolled away and the ampoule cooled. The arsenic boat and quartz sealing plug are moved into place by manipulating the magnetic stainless steel plug with an external magnet so that the ampoule after sealing is 55 cm long. The ampoule is sealed and the GaAs synthesized by placing the ampoule into the two zone gradient freeze furnace. The composition of the melt is fixed by maintaining an arsenic reservoir at 620°C. The high temperature end of the furnace is controlled automatically and the melt is allowed to soak for 6 hours at temperature (1236°C). A motor driven set point controller then reduces the temperature to an effective growth rate of 1.25 cm/hr. Care is taken to prevent overshoot during the heating cycle to avoid melting the seed crystal. When the hottest portion of the ampoule has cooled to 1200° C the high temperature furnace is turned off. The arsenic pressure reservoir is maintained at

620°C until the high temperature furnace has cooled sufficiently to produce a "cool spot" of 600°C midway in the furnace. The arsenic reservoir furnace is then turned off and the quartz tube removed and allowed to cool at room temperature.

Electrical Properties

Forty-nine ingots of GaAs have been compounded in PBN by the method just described. Thirty-four of these ingots were semi-insulating 1" from the first end to freeze. Five of the ingots that were not semi-insulating were traced to a contaminated lot of arsenic. It has not been possible to determine why the other ten ingots were not semi-insulating. The non semi-insulating ingots appear to be n-type but the Van der Pauw measurements were so ambiguous that they could not be analyzed. The conductivity between the various contacts indicated a very inhomogeneous material. PBN compounded GaAs is very polycrystalline and it is not possible to select single crystal areas for electrical measurements.

It is evident that a clear picture of the impurity concentration cannot be found by looking at the electrical data on the polycrystalline ingots. A series of single crystals were pulled using semi-insulating charge material, conducting charge material and semi-insulating charge material with known Te additions. These results are discussed in the following section on LEC growth of PBN-GaAs.

II. GaAs Single Crystal Growth by Liquid Encapsulation Czochralski (LEC)

Introduction

In NRL Memorandum Report #3360 we described the procedure we have used to convert the high purity PBN GaAs to single crystals suitable for use as substrate material. Since copies of NRL Memo Report #3360 are no longer available we will again describe the crystal growth procedure we have used.

Since the last annual report we have refined the procedure slightly and identified the important growth parameters that lead to consistent high quality crystals. The GaAs crystals have been analyzed for purity, crystalline perfection and FETs have been made using both liquid phase epitaxy and vapor phase epitaxy.

Apparatus and Procedure

The Czochralski crystal puller, power source and associated equipment are shown in Fig. 3. Except for the PBN crucible the experimental arrangement is fairly standard throughout the industry.

At the present time we have identified several things in the apparatus which are critical to achieving reproducible results in single crystal growth. The first requirement is an R.F. generator and controller capable of delivering and maintaining a constant, reproducible amount of R.F. power. We have used R.F. generators with saturable reactor control from three manufacturers with equal success. All of these generators have internal power controls capable of accepting a 0-5 ma control current. We have used an L&N AZAR controller throughout this program but probably any controller meeting or exceeding the specifications of the L&N equipment would be suitable. We

have used the controller in the automatic mode and made any power adjustments by changing the zero suppress. The crystal puller is equipped with both seed and crucible rotation. We have found that crucible rotation is essential for reliable single crystal growth and low dislocations.

The procedure for a crystal growth run is as follows:

The day prior to the crystal growth run a pellet of B_2O_3 is vacuum baked in a Malvern Czochralski puller. A 30 gram pellet of B_2O_3 (99.999% pure from Yamanaka Chemical Ind. Ltd., Japan, purchased from A. D. Little, Inc.) is placed in a PBN flat bottom crucible purchased from the Carbon Products Div., Union Carbide Corp. The crucible and B_2O_3 are placed in the crystal puller and evacuated to a pressure of 50 millitorr. The system is then backfilled to 10 psi pressure above atmospheric with 99.995% pure argon that has been passed through a model 2-B gettering furnace from Centorr Associates Inc. The system is again evacuated and backfilled with argon. The argon is allowed to flow maintaining a positive pressure of 10 psi. The system is then heated by a graphite susceptor and a 15 kw R.F. generator (frequency = 400 kc). The heating is controlled by an R.F. pickup coil giving a feedback to a Leeds and Northrup Series 80 Controller. The controller is on the manual mode and is adjusted so that the crucible is heated to $1200^{\circ}C \pm 50^{\circ}C$. The system is slowly evacuated with the evacuation rate being determined by the amount of bubbling that occurs. The evacuation rate is controlled so that the B_2O_3 does not bubble over the top of the crucible. The amount of bubbling and the time required before the system can be fully open to the mechanical vacuum pump varies with each B_2O_3 pellet even though the pellets are from the same lot. The B_2O_3 is baked over-night fully open to the vacuum pump to insure that the B_2O_3 is as dry as possible.

The polycrystalline PBN GaAs charge is sawed into pieces 2.5 cm in length so that when the pieces are stood on end, they fill the PBN crucible to a depth of 2.5 cm with as few voids as possible. A close fit is desired so that when the GaAs is placed on top of the B_2O_3 and heated, the GaAs will sink to be completely covered by the encapsulant. After sawing, the GaAs pieces are etched in a 5% bromine-methanol solution for 5 minutes, then dried over-night in a drying oven. The GaAs seed crystal is etched for 3 minutes in the 5% bromine-methanol solution and dried for 30 minutes in the drying oven. After etching, the (111)A face appears rough, whereas the (111)B face appears smooth and polished. The seed is mounted so that the (111)B face will be in contact with the melt and the seed and seed holder stored in the drying oven overnight.

The next day, the vacuum pump is valved off of the dried B_2O_3 and argon is backfilled and allowed to flow at 10 psi positive pressure. The R.F. generator is turned off and the system is allowed to cool to room temperature under the flowing argon. The GaAs seed is mounted on the top pull rod of the Czochralski crystal puller. The etched GaAs charge is weighed and any desired dopants are calculated and weighed. The charge and dopant are placed in the PBN crucible on top of the solidified B_2O_3 so that when the B_2O_3 melts the GaAs will sink to be completely covered by the B_2O_3. The loaded crucible is placed into the graphite susceptor in the crystal puller as shown in Fig. 4. The puller is twice evacuated and backfilled with dry argon. The argon is 99.9995% pure from Matheson Gas Products, Lyndhurst, New Jersey and passed through a Matheson Model 450 purifier and Model 451 cartridge. The power is controlled by an R.F. pickup coil giving backfeed to a Leeds and Northrup Speedomax W Recorder, Calibrated Azar, and Series 80 Controller. The heater is placed on automatic control and is brought

rapidly to a temperature slightly above the melting point of GaAs. The pieces of GaAs quickly sink through and are completely covered by the molten B_2O_3 minimizing loss of arsenic. After the GaAs has melted, the seed is brought into contact with the melt and allowed to equilibrate for 10 minutes. The temperature is then lowered to growth conditions and pulling is begun. Diameter control is accomplished by observation of the growing crystal and adjustment of the Azar.

Pull rates from 2.0 to 2.5 cm have been used with the seed rotating clockwise at 0 to 3 rpm and the crucible also rotating clockwise at 5 to 10 rpm. Only the (111)B seed orientation has been used. The B_2O_3 depth is 8 mm and the GaAs charges weigh 130 to 150 grams.

As described previously we have been using a R.F. heating coil mounted outside a quartz reaction chamber and a graphite susceptor which also acts as a support pedestal for the PBN crucible. We have found that for any given size of crucible and a fixed weight of charge material there is an optimum height of the susceptor which will result in a high yield of single crystal GaAs with good crystallinity (Fig. 4). For example, if the susceptor were at point A or higher in Fig. 4 the grown crystal will be too hot and arsenic loss from the surface will be so great as to cause gallium droplets to form on the surface and then move into the interior of the crystal as growth proceeds. When the susceptor height is near point B seed on is easily accomplished, the crystal tapers out to the desired diameter easily and the entire charge is converted to a single crystal with low dislocation density ($1\text{-}5 \times 10^3$ dislocations cm^{-2}). A typical crystal is shown in Fig. 5. When the susceptor is at position C, it is difficult to get a good seed on and the crystal diameter expands rapidly frequently leading to poly-crystalline growth. The effect of raising or lowering the susceptor height

with respect to a fixed charge of GaAs is to adjust the temperature profile in the growing crystal and thereby adjusting the shape of the solid liquid interface. It is obvious from experience that when the susceptor is at position B the growth interface is either flat or convex into the melt. In fact it is more likely that the growth interface is convex into the melt since the star etch pit pattern that results from slip when the exterior of a growing crystal cools much more rapidly than the interior has never been observed in our crystals. When the thermal geometry of the system is properly adjusted for high yield the B_2O_3 does not adhere to the growing crystal. There is always a loss of some arsenic from the crystal surface but it is not a serious problem. Raising or lowering the R.F. coil with respect to the susceptor can also change the thermal geometry of the system. This effect is not as dramatic as raising or lowering the susceptor height and we have found that it is more advantageous to keep the R.F. coil low, thus putting more heat in from the bottom of the melt. When more heat is introduced at the bottom of the melt fewer power changes are required to maintain a constant diameter crystal as the melt is depleted. Using the arrangement just described the entire melt can be pulled. This results in less damage to the PBN crucible.

PBN crucibles have been used throughout this work. They have been used to prevent possible contamination of the melt from impurities in a quartz crucible which could result from the B_2O_3 dissolving the quartz during the crystal growing run. The 2 inch diameter PBN crucibles have been extremely durable during this investigation. One crucible for instance has been subjected to 40 heating and cooling cycles and is still usable. Some PBN spalls after each crystal growth run. Since PBN is a layered

material this spalling does not affect the integrity of the crucible. Only two PBN crucibles have been destroyed during the course of this investigation and in each case they were crucibles which showed evidence of bowing in the bottom of the crucible prior to use. Also in both of these cases 1.4 cm height of B_2O_3 was used instead of the usual 0.9 cm height.

Crystal Perfection - Dislocation density of the crystals have been determined using a standard Richards and Crocker etch on the 111B surface. The dislocation density observed is usually 10^3 - 5 x 10^3. No lineage has been observed and the dislocations are randomly spaced. The etch pits are much smaller than those seen in gradient freeze grown GaAs crystals. Dr. T. J. Magee of the Stanford Research Institute examined several of our LEC GaAs crystals. He wrote,

> Somewhat earlier you forwarded to us four single crystal slices of (100) orientation GaAs grown at NRL. Captain Wayne Anderson of WPAFB also sent similar NRL samples to us for evaluation. Using transmission electron microscopy/transmission election diffraction, we examined 20 samples (II-40L, II-35L) prepared from the supplied material. The data obtained from these experiments indicated an apparent absence or low density of microscopic defects. Maximum dislocation densities were in the range, 10^3 cm^{-2}. The majority of specimens examined, however, exhibited defect densities less than $10^3 cm^{-2}$. As a matter of reference, GaAs samples from other sources showed relatively high microscopic defect densities, often exceeding 10^{12} cm^{-2}, as described in our WPAFB contract report. Your samples are perhaps the best I have seen over the past five years.

Undoped PBN-LEC GaAs

A number of undoped, lightly tellurium doped and lightly chromium doped PBN-LEC crystals have been grown. When one analyzes the electrical properties of these crystals as a function of fraction solidified a consistent pattern begins to emerge. This pattern suggests that undoped PBN-LEC GaAs is semi-insulating because the electrical properties are dominated by a deep donor (probably oxygen). In Fig. 6 the resistivity as a function of fraction

olidified has been plotted for three undoped PBN-LEC crystals. The crystals re semi-insulating over half of their length and then turn conducting p-ype. In Fig. 7, two chromium doped crystals are plotted. If one compares igs. 6 and 7 we see that the electrical properties are essentially unchanged. he last fifty percent of the crystal is still dominated by shallow acceptors nd no amount of chromium will make the material semi-insulating. In Fig. 8 he resistivity of three tellurium doped crystals is plotted as a function f fraction solidified. Again we see that for tellurium additions of 1 nd 2 x 10^{15} atoms cm^{-3} the electrical properties of the crystal are unchanged from that of the undoped and chromium doped crystals indicating that the shallow acceptors still exceed the shallow donors and the semi-insulating character of the beginning of the crystal is determined by a deep donor compensating the excess shallow acceptor concentration. In Fig. 8 the resistivity of a third crystal is also plotted. When 4 x 10^{15} Te atoms are added the crystal is n-type and conducting at both room temperature and nitrogen temperature. This would fix the net acceptor concentration at the beginning of the crystal at less than 4 x $10^{15} cm^{-3}$. Our information to date would show that undoped PBN-LEC GaAs is dominated by a deep donor (oxygen). Our information at present does not indicate the amount of oxygen present at the beginning of the crystal. It also does not indicate whether the oxygen is decreasing toward the middle of the crystal or whether the excess shallow acceptors are increasing while the deep donor concentration is remaining constant throughout the crystal. Additional experiments with controlled additions of a shallow acceptor impurity will be required to educe the initial deep donor concentration. Also controlled additions f oxygen will be attempted to confirm the validity of the proposed model.

As mentioned before, the polycrystalline PBN charge material is either semi-insulating or slightly conducting with carrier concentrations up to 2.5×10^{17}. It is not uncommon to have apparent carrier concentrations that are several orders of magnitude too high when material is very closely compensated, inhomogeneous, or has p-n junctions between the hall contacts. To test whether our PBN material with the anomalous conductivity fits into this category we pulled two PBN-LEC undoped crystals. In one case, IV-13L, only semi-insulating charge material was used. In IV-7L only conducting charge material was used. Table I summarizes the electrical properties of the charge material. In Fig. 6 the resistivity vs. fraction solidified for IV-7 and IV-13 have been plotted. As can be seen there is virtually no difference in the electrical properties of the two crystals. One must reluctantly conclude that electrical evaluation of the compounded PBN-GaAs is not a meaningful measure of the material's purity.

Table I

Electrical Properties (300K) of PBN-GaAs Charge Material

	ρ (ohm-cm)	$N_d - N_a$ (cm^{-3})	μ ($cm^2 V^{-1} s^{-1}$)	Type
		IV-13L		
10-127 S	9.3×10^7	1.5×10^7	4250	n
10-129 S	4.4×10^8	1.8×10^8	78	n
10-131 S	9.4×10^7	1.6×10^7	4275	n
		IV-7L		
10-113 S	47	8.1×10^{15}	16	n
10-115 S	99	2.9×10^{15}	2	p
10-121 S	759	5.9×10^{14}	14	n

Stabilization of Semi-insulating GaAs in LPE Process

During the liquid phase epitaxial (LPE) growth of GaAs on a semi-insulating substrate, the interface of the substrate under the grown layer often becomes conductive, usually described as "converted." The thickness of the "converted" layer depends on the duration of heating the substrate. The "converted" layer is usually p-type. The difficulties in fabricating devices on a S.I. substrate lie in the fact that a substrate from one ingot may prove to be stable under a thermal cycle of LPE process, while another substrate from another ingot may not. There is, so far, no formula for the crystal growth process which assures the outcome of a stable GaAs crystal during the LPE. As a result, the grown crystals are put to a variety of heating tests and the ingots are accepted and rejected for further processing into devices according to the results of the various tests. The causes of the "converted" layer are not exactly certain and the theories to explain them are legion. Since we know that loss of arsenic cannot be prevented unless an arsenic overpressure is used we have attempted to grow a S.I. GaAs crystal with the proper balance between shallow donors, shallow acceptors, deep acceptors and possibly deep donors that will prevent the formation of acceptor complexes or overcompensate any acceptor complexes that are formed.

The approach that has been taken is to add sufficient tellurium to our PBN compounded GaAs to assure that the electrical properties were dominated by a shallow donor (Fig. 7). Tellurium was selected to avoid possible complications that might arise from the use of amphoteric elements such as silicon or tin. Having determined that 4×10^{15} tellurium atoms

cm^{-3} was the lower limit, we then added various amounts of tellurium and a sufficient amount of the deep acceptor chromium to compensate the net donor concentration. We varied both the tellurium concentration and the chromium to tellurium ratio. Table II summarizes our results. The results to date are encouraging but not conclusive. Of the five crystals prepared only one failed our "qualification test."

TABLE II

Crystal #	Before Heating ρ (ohm/□)	After Heating ρ (ohm/□)
III-16L Cr-3×10^{16} Te 6×10^{15}	4.6×10^{9}	4.6×10^{9}
III-28L Cr 5×10^{15} Te 4×10^{15}	7×10^{9}	1.6×10^{6}
III-59L Cr 3×10^{16} Te 1×10^{16}	1.9×10^{9}	1.5×10^{8}
IV-55L Cr 2×10^{16} Te 6×10^{15}	2.4×10^{10}	5.6×10^{9}
IV-77L Cr-4×10^{16} Te-6×10^{15}	6.5×10^{9}	3.4×10^{9}

Our "qualification test" consists of preparing a (100) substrate for an epitaxial growth run. The preparation is described in the subsequent section on "Liquid Phase Epitaxial Growth." The substrate is heated in

our liquid epitaxial reactor for 90 minutes at 750°C. The sheet resistivity is determined by Van der Pauw measurements at room temperature before and after heating.

It is clear from the results of III-28L that a low net donor concentration and a small chromium to tellurium ratio is not satisfactory. The most stable crystals were found to have Te and Cr concentrations of 6-10 x $10^{15}cm^{-3}$ and 2-4 x $10^{16}cm^{-3}$, respectively.

In addition to the thermal heating tests various other properties of the Cr-Te doped crystals have been examined. Photoluminescence measurements have shown that the defect band at 1.413 eV is present in the heated samples even though the surface is not conducting. In addition several photoluminescence peaks appear in the Cr-Te material that do not appear in commercial Cr doped semi-insulating GaAs. (See the companion NRL Memorandum Report on characterization.)

An additional complicating factor appears from the EPR results obtained by Krebs and Stauss (Code 6440).[4] The amount of Cr^{2+} (the compensated chromium state) that they observed exceeds the amount of Te added by a factor of approximately 2.5 to 1. This result is not consistent with the normal picture of Cr compensation of donors in GaAs. This point needs clarification and will be a subject for investigation during the following year.

Thermal conversion tests were also performed on slices of III-16L by Dr. G. S. Kamath of Hughes Research Laboratories. He found that there was no surface conversion at temperatures up to 780°C for 2 hours. He did find an n-type skin at 800°C which became substantial at 835°C. Dr. Kamath did state that this result was better than 75% of the commercial substrates that he had seen. He also attempted to grow a 5x$10^{15}cm^{-3}$

n-type layer on these substrates. The grown layer was measured to have a carrier concentration of 2 x 10^{16} and a low mobility of 2000 $cm^2v^{-1}sec^{-1}$. This could indicate a conversion layer which was not observed in the electrical evaluation. This investigation will be pursued further with substrates of different dopant concentrations.

FET device results were obtained on three liquid phase epitaxial experiments using Cr-Te doped substrates. In the first case the layer was grown in-house by Dr. P.E.R. Nordquist using the Ga-etch procedure. The material was processed at Hughes Research Labs. by Dr. C. F. Krumm into 0.5 micron gate FETs. The results of these tests are described in detail in the subsequent section of this report under "liquid phase epitaxy." The devices made showed typical low noise characteristics and excellent gain at 10 GHz. In view of the small size of the wafer and the limited number of devices evaluated the result was encouraging.

Dr. Masahiro Omori, Manager of Device Development at Avantek Corp., arranged to grow FET layers by LPE directly on substrates from III-59L and IV-55. One half-micron FETs were prepared. The results on III-59L were not encouraging. They were unable to pinch off the devices indicating that a conducting layer had formed at the epi-layer substrate interface. The slices they used were from the bottom of III-59L which was not as good electrically as the top slices or as good as III-16L.

Avantek subsequently grew device quality LPE layers on slices of IV-55L (Cr 2 x 10^{16} and Te 6 x 10^{15}). The device results indicated a small but detectable amount of conversion at the substrate-active layer interface. The RF performance of their 0.5 gate FET at 6 GHz was 1.9 dB noise and a 10.5 dB associated gain. This result is very encouraging and this will be pursued during the coming year. Larger Cr to Te ratios seem to be indicated.

Experimental Results - GaAs single crystal wafers have been sent to various industrial laboratories for specific tests and also processing into FET devices. From the results to date it would appear that whereas some substrates are suitable for one process they may not be suitable for another process (i.e. ion implantation, vapor phase epitaxy, liquid phase epitaxy).

Ion Implantation - High purity undoped slices of PBN-LEC GaAs have been evaluated at Hewlett Packard Laboratories and at the Science Center, Rockwell International. At Hewlett Packard Laboratories (HP) wafers from crystals II-35L and II-40L were subjected to their qualification test which involves capping an unimplanted wafer with Si_2N_3 and annealing for 15 minutes at 850°C. The wafers did not show surface conversion, i.e., the sheet resistance of the annealed slices was greater than 10^8 ohm/□. HP then implanted several wafers with Se using their standard procedure. The carrier concentration and the implant profile were normal. The 77K carrier concentration was 2×10^{17} cm^{-3} and the mobility was 4600 $cm^2V^{-1}S^{-1}$. They said "the surface morphology of the annealed wafers is good and would be suitable for MESFET fabrication." No FETs were prepared.

At Rockwell, wafers from the same two crystals were evaluated (II-40L and II-35L) using their standard qualification tests. The wafers passed both their Si_2N_3 cap and anneal test and their Kr bombardment test. They are processing the remaining material into FETs. The results are not yet available.

Vapor Phase Epitaxy - Both undoped and Cr-Te doped wafers have been evaluated for use as VPE substrates at Bell Telephone Labs., Raytheon Labs. and Lincoln Labs. At Bell Telephone Labs. and Lincoln Labs. they found that the fast diffusing acceptor usually present in S.I. GaAs was still present. This fast diffusing acceptor degrades the quality of the buffer layer at the

substrate buffer layer interface. A recent result at Raytheon Laboratory indicates that by proper control of the arsenic/gallium ratio when growth is initiated the unknown acceptor diffusion can be suppressed or masked when using a Cr-Te doped S.I. wafer. Raytheon Laboratories prepared both buffered and unbuffered small signal 1 micron FET devices on NRL Cr-Te doped samples (III-16L). Both types of FETs had minimum noise figures of 2.1 to 2.3 dB at 6 GHz with associated gains between 8.5 and 10 dB. For a more complete evaluation of these results see the characterization portion of this program edited by B. D. McCombe, Code 5270.

Summary and Recommendations

It has been shown that undoped PBN-LEC GaAs can be produced consistently. The defect density in LEC crystals can be very good. Undoped PBN-LEC GaAs substrates are very promising for ion implantation and VPE when an in-situ etch of the substrate is used. A model indicating oxygen as the deep center which determines the S.I. character of the material has been proposed. Efforts to intentionally introduce oxygen will be attempted to increase the yield of S.I. GaAs in each crystal.

Considerable progress has been made toward obtaining a thermally stable S.I. GaAs substrate that is reproducible. Additional Cr-Te ratios are indicated. Also other dopants such as Sn will be investigated.

III. InP - Compounding and LEC Growth

Introduction

Recent work indicates that the $Ga_{1-x}In_xP_{1-y}As_y$ quaternary alloys grown on InP substrates have material properties that are desirable for applications in microwave[5,6] as well as optoelectronic[7] devices. A major limitation on (In,Ga) (As,P)/InP or other structures requiring InP substrates is the inferior quality and limited availability of InP substrates (relative to GaAs substrates).[7] Alleviation of the InP substrate problem requires progress in four areas. First, a technique to reproducibly synthesize high purity bulk InP must be devised. Secondly, the parameters affecting defect density and twinning during bulk crystal growth need to be understood and controlled. Thirdly, the segregation coefficients and solubility limitations of dopants must be known so that electrical properties can be controlled while introducing neither strain in the crystal nor precipitation of second phases. Fourthly, proper handling techniques need to be developed for the sawing and polishing of the brittle InP substrates. This report discusses the techniques employed and results obtained in the above areas of research at NRL.

Synthesis

A large variation in the purity of charge material causes great difficulty in controlling the electrical properties of the resulting single crystals. Since the purity of commercially available polycrystalline InP varies widely from supplier to supplier and from lot to lot, the development of a technique to reproducibly synthesize high purity bulk InP has been necessitated. The method of synthesis being studied involves compounding from the elements in a pyrolytic boron nitride (PBN) boat using the gradient freeze technique. PBN ware has been used because of its successful application in the synthesis of high purity GaAs[8] and because Bachmann[9] reported that InP synthesized in

a PBN boat was of higher purity than InP synthesized in either silica or carbon boats. The experimental apparatus, procedure, and results are discussed below.

Synthetic Procedure

Approximately 75 g of indium (6-9's purity purchased from Cominco) in a PBN boat are vacuum baked for 20 hours at 700°C. The indium is cooled to room temperature under vacuum and transferred to a clean silica tube (I.D. = 30 mm, O.D. = 34 mm, length = 762 mm). A silica boat containing red phosphorus (Alusuisse semiconductor grade or M.C.P. 6-9's purity) in sufficient quantity for compounding and maintenance of pressure is placed in the compounding ampoule. The ampoule is evacuated (pressure $\leq 5 \times 10^{-7}$ torr), sealed, and placed in a two-zone conventional gradient freeze furnace. The furnace is heated to the conditions shown in Fig. 1. During the warm-up, care must be taken to avoid large over-shoots of the temperature which result in increased phosphorus pressure and could lead to breakage of the silica ampoule. The phosphorus pressure is controlled by the temperature of the coldest end of the tube and is calculated using the pressure-temperature relationship published by Bachmann.[10] The hot end of the tube is in a temperature gradient of 60°C across the length (12.5 cm) of the PBN boat. The temperature conditions of Fig. 9 are maintained for five hours, after which a motor driven set point controller reduces the temperature of the hot end yielding an effective growth rate of 0.17 cm/hr at 8 atmospheres of pressure or 0.34 cm/hr at 15 atmospheres of phosphorus pressure. After the temperature of the PBN boat has been reduced to 1030°C, both zones of the furnace are turned off. The ampoule is removed from the furnace when the temperature of the cold zone falls to 400°C (1.5 atmospheres of phosphorus pressure).

Synthesis Results

The top surface of the boules are homogeneous in appearance but excess indium tends to collect at the bottom of the boule and at the grain boundaries on the last 2 or 3 cm to freeze (Figure 10). The presence of excess indium results in slight sticking between the PBN boat and boule. The end of the boule that is free of excess indium does not exhibit the sticking problem. Inserting the boat and boule in an ultrasonic cleaner for a few minutes usually frees the boule from the PBN boat. The boules are polycrystalline and a single grain is sectioned out for Hall measurements. Samples for the electrical measurements are taken at 2.5 cm intervals across the length of the boule. Figure 11 shows a plot of N_d-N_a versus location in the boule. Because N_d-N_a tends to exceed $10^{16}/cm^3$ in the last 2.5 cm of the boule, only the first 80% of each boule is used for Czochralski growth.

Table I and Figure 12 contain N_d-N_a and mobility values measured at 77K using the Van der Pauw technique. In each case the measurements were in samples taken 2.5 cm from the first end to freeze. Figure 12 plots mobility at 77K against N_d-N_a for several compensation ratios[11] plus data points from this work. The data in Table I and Figure 12 indicate that the purity of the InP boules synthesized at 15 atmospheres in PBN boats is not significantly different from the purity obtained at 8 atmospheres using PBN boats. However, as the phosphorus pressure is reduced, the growth rate must also be reduced to avoid inclusions of excess indium. For the experiments performed at 8 atmospheres of pressure, the purity of the compounded material was affected by the type of boat material. The use of PBN boats resulted in higher purity InP than was obtained using silica boats. Although higher purity when PBN boats are used is consistent with results published by Bachmann,[9] we plan to do several experiments using high purity spectrosil silica boats for further comparison.

Growth of Single Crystal InP

The liquid encapsulated Czochralski (LEC) technique is the most extensively used method for growth of bulk single crystal InP. The principal obstacle to expeditious growth of large single crystal InP by the LEC method is the phenomenon of twinning. When grown in the (111) direction, InP crystals usually attain a cross section that is triangular in shape. One type of twin tends to develop at the apexes of the triangle where (111) facets are located. As growth continues, this type of twin follows the (111) plane deeper into the crystal. The second type of twin seems to occur at a random location on the periphery of the growing crystal and may be related to the presence of impurities at the B_2O_3 melt interface. This type of twin generally does not penetrate deeply into the crystal but remains near the periphery as growth is continued. Certain precautions, including the careful cleaning and etching of the InP charge to remove oxides and a thorough drying of the B_2O_3 to prevent scum formation,[12] reduces the incidence of the second type of twin. Parameters affecting defect density and twinning at (111) facets along (111) planes need further understanding in order to maximize crystalline quality and availability of InP substrates.

The problem of purity of charge material and avoidance of contamination during the LEC growth process has been the second major obstacle to production of semi-insulating InP substrates. Cr-doped InP typically has a room temperature resistivity of 10^3-10^5 ohm-cm and Cr is soluble to .3 wt % in the melt giving 10^{16} Cr atoms/cm^3.[13] Whereas Fe-doped InP has a room temperature resistivity $\geq 10^7$ ohm-cm,[15] and Fe has a maximum solubility of .3 wt % in the melt,[16] the segregation coefficient had not been previously published. Knowledge of the segregation coefficient would allow calculation of the minimum

concentration of iron required in the melt in order to compensate the excess donors present in the charge material. Reducing the dopant concentration may avoid strain in the doped crystal that is thought to be associated with high dopant concentrations, and would preclude precipitation of second phases until after a large percentage of the melt had been pulled.

This section of the report contains a summary of the procedures used as well as the results and discussion of numerous crystal growth and doping experiments.

LEC Procedure

Thirty grams of B_2O_3 in a PBN crucible are vacuum baked overnight then cooled to room temperature under flowing gettered argon. Approximately 150 g of InP, that has been previously etched and dried, are placed (along with any desired dopants) in the PBN crucible on top of the solidified B_2O_3. The high pressure furnace (Figure 13) is evacuated and backfilled with high purity argon to 30 atmospheres of pressure. After the B_2O_3 and InP charge are melted, crystal growth proceeds using pull rates that have ranged from 1.7-2.5 cm/hr. The seed is rotated (0-2 rpm) in the same direction as the crucible (5-10 rpm). A more detailed description of the vacuum baking and growth procedures may be found in reference 8.

Crystal Growth Results

During InP crystal growth, the B_2O_3 remains clear and scum free. Bachmann et al.[14] have reported that the exclusion of any residual water was found to be extremely important to establish a clean scum-free B_2O_3 melt interface during InP growth. The use of PBN crucibles and the in-situ vacuum baking of the B_2O_3 has eliminated the scum formation and has helped to reduce the incidence of one type of twinning problem. The clearness and lack of color of the B_2O_3 during and after crystal growth are indications that neither

the melt nor the crucible are being chemically attacked. Several LEC crystals have been grown, without intentionally adding any dopant, and their carrier concentrations and mobility values have been compared to those of the charge material (Table I). Since the electrical properties of the undoped LEC crystals are not significantly different from those of the charge material, the PBN crucibles are not contaminating the LEC crystals with electrically active impurities. Photoluminescence data (Figure 14) on undoped LEC crystal #1-81-H have identified one acceptor impurity, zinc. The photoluminescence peak for zinc was also identified in the charge material. The photoluminescence data did not provide any information concerning the concentrations of the acceptor impurity nor have the donor impurities been identified.

Mizuno and Watanabe[15] have reported that InP doped with 1500 ppm by Fe wt. Fe in the InP melt produced semi-insulating InP with a room temperature resistivity $\geq 10^7$ ohm-cm, but have published data on neither solubility limitations nor the segregation coefficient of Fe in InP. The high purity charge material being synthesized at NRL and the use of the non-contaminating LEC process provides an opportunity to study the effects of dopant concentration on the production of semi-insulating substrates. Workers at NRL and at NSWC have determined that Fe is soluble in the InP melt to .3 wt %.[16] EPR measurements were used to determine the Fe^{3+} concentration in a p-type InP crystal (1-45-H) at a point just above where the precipitation of the second phase occurred. The Fe^{3+} concentration was $2.5 \times 10^{17}/cm^3$,[17] yielding an effective segregation coefficient of 1.6×10^{-3}.[15] Several additional experiments have been done to verify the effective segregation coefficient. Crystal #1-66-H was grown using charge material that was n-type ($N_d-N_a = 8 \times 10^{15}/cm^3$) and was doped with Sn (to give 4×10^{16} Sn/cm^3) and Fe (to give 1.3×10^{16} Fe/cm^3). Crystal #1-66-H was expected to be n-type with $N_d-N_a = 3.5 \times 10^{16}/cm^3$ and

was measured to be n-type with N_d-N_a = 3.2 x $10^{16}/cm^3$. Crystal #1-74-H was grown using a melt doped with 800 ppm by wt. Fe while crystals #1-85-H, 1-91-H, and 1-94-H were doped at 150 ppm by wt. Fe in the melt. In each of the 5 crystals, the resistivity was greater than 10^7 ohm-cm (Table II) and did not vary as a function of Fe concentration. The Fe^{3+} concentration in 1-91-H was determined by EPR to be 1.9 x $10^{16}/cm^3$ which is consistent with the Fe^{3+} concentration expected for a segregation coefficient of $1.6x10^{-3}$.

Table III compares data concerning Cr and Fe as dopants in InP. The dopants have solubility limitations in the melt that are nearly identical, but the segregation coefficient of Fe is an order of magnitude larger than that for Cr. Fe-doping can therefore compensate material that has donor concentrations much higher than can be compensated by Cr-doping. The fact that Fe-doping produces a resistivity which is several orders of magnitude higher than that produced by Cr-doping may have important implications concerning the choice of dopant for FET or TED device substrates. The data in Table II are evidence that when high purity charge material is available, semi-insulating InP can be grown consistently by adding only a small amount of Fe to the melt. Use of small amounts of dopant may be of importance for devices produced by ion implantation, as well as devices produced by epitaxial growth.

Summary

An experimental procedure for synthesizing bulk InP has been developed to produce high purity charge material for LEC crystal growth. The procedure described in this report produces InP charge material with N_d-N_a at mid $10^{15}/cm^3$ and with 77K mobility values as high as 45,700 cm^2/vs. The charge material has been doped with Fe to grow semi-insulating LEC InP crystals and the effective segregation coefficient of Fe in InP has been determined to be 1.6 x 10^{-3}. Knowledge of the segregation coefficient along with the availability of the

high purity charge material has permitted the Fe concentration in the LEC crystals to be lowered to approximately $10^{16}/cm^3$ and still consistently produce semi-insulating InP. The procedure used for the LEC growth of InP has reduced but has not eliminated the incidence of twinning. The problem of twinning needs further understanding in order to increase the availability of InP substrates.

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TABLE I

Hall Measurements on InP

Boule	Boat	$(N_d-N_a)_{77}(cm^{-3})$	$\mu_{77}(cm^2/Vs)$	Pressure
Syn #9	BN	2.3×10^{15}	39,800	15 Atm.
Syn #10	BN	2.1×10^{15}	27,600	15 Atm.
Syn #12	BN	2.4×10^{15}	45,700	15 Atm.
Syn #14	BN	4.7×10^{15}	26,300	15 Atm.
Syn #15	BN	5.2×10^{15}	24,900	15 Atm.
Syn #27	BN	4.9×10^{15}	30,400	10 Atm.
Syn #28	BN	3.6×10^{15}	33,500	10 Atm.
Syn #20	BN	3.8×10^{15}	28,480	8 Atm.
Syn #21	BN	4.5×10^{15}	25,600	8 Atm.
Syn #17	SiO_2	2.0×10^{16}	9,840	8 Atm.
Syn #18	SiO_2	1.1×10^{16}	13,670	8 Atm.
Syn #19	SiO_2	1.6×10^{16}	10,820	8 Atm.

TABLE II

Fe-Doped InP

Crystal	Fe (wt.%)	ρ (ohm-cm)
1-26-H	.15	$> 10^7$
1-74-H	.08	$> 10^7$
1-85-H	.015	$> 10^7$
1-91-H	.015	$> 10^7$
1-94-H	.015	$> 10^7$

TABLE III

Dopants for Semi-insulating InP

	M = Fe	M = Cr
M_{max} in melt	0.3 wt. %	0.3 wt. %
M_{max} in crystal	$2.5 \times 10^{17}/cm^3$	$2 \times 10^{16}/cm^3$
K_{eff}	1.6×10^{-3}	1.1×10^{-4}
Resistivity	10^7 ohm-cm	10^3-10^4 ohm-cm

IV. Liquid Phase Epitaxial Growth of Gallium Arsenide

Introduction

The general goal of the GaAs Liquid Phase Epitaxial (LPE) program has been to grow layers of GaAs suitable for Field Effect Transistor (FET) applications. These layers must be thin (2000-3500Å), n-type (1-2 x 10^{17}carriers cm^{-3}), grown on semi-insulating GaAs substrates with a flat surface uniform enough to permit device fabrication. The program aspires to an understanding of the growth process and those variables which control it so that the knowledge gained in GaAs layer growth can be readily transferred to the epitaxial growth of other materials (e.g., InP, and ternary and quaternary III-V compounds).

The general conditions for the growth of high quality epitaxial layers may be summarized as follows:

(1) The substrate surface must be uniform and featureless since surface imperfections will be replicated in the grown layer.

(2) The substrate surface must be free from impurities and must be conducive to uniform, widespread nucleation of the grown layer.

(3) The substrate surface must be free from imperfections which affect the electrical properties of the layer e.g. an electrically type converted layer on the surface. Surface type conversion and the presence of interface states degrade electrical properties of the fabricated devices.

Growth of device quality epitaxial layers by the LPE process offers the advantages of being conceptually and mechanically simple in both operation and equipment design. A continuing problem has been damage to the substrate surface during the pregrowth heating and bakeout period. The damage may be both morphological (roughness) and electrical (surface conversion layer). Growth of a buffer layer between substrate and active layer has been the usual way to minimize the effects of thermal damage.

This report summarizes LPE studies done using a gallium etch of the substrate surface before epi layer growth. The gallium etch, by dissolving an appreciable portion of the substrate surface immediately prior to layer growth, removes the thermally damaged and electrically converted layers of the substrate leaving a uniform, clean surface for subsequent epi layer growth. The need for a buffer layer between substrate and active layer has been minimized or eliminated thus simplifying the growth procedure and offering economic and processing advantages. The epitaxial layers grown upon this freshly etched surface are flat and uniform, and have been processed into FETs having excellent electrical properties.

Early work using the Ga etching technique has been reported;[18,21] the present work refines and extends the procedures and discusses those variables critical for production of high quality epitaxial layers.

Experimental

Equipment and Materials

The LPE experiments were conducted in a quartz tube having a stainless steel end cap enclosing an atmosphere of flowing (0.4 lpm) palladium diffused hydrogen. The tube is heated by a movable heat pipe furnace which permits rapid cooling of the grown layers and fast turn around between experiments. Furnace temperature is controlled through external circuitry and is stable to $\pm$ 0.1^{o} in the growth zone.

The epitaxial growth reactor (Fig. 15) is contained within the quartz tube and is machined to specification from high purity graphite and purified by the manufacturer. The graphite is dense and close grained and is not wet by gallium during the growth operations. The graphite reactor has two square wells, one for a gallium etch solution and one for the growth melt. A movable graphite slider forms the bottom of the wells and accommodates, in separate

depressions, a high purity GaAs source wafer and a polished substrate. Clearance between the bottom of the graphite block and the wafers is adjusted by using spacers of different thickness. A clearance of between 0.003" and 0.004" seems optimum for the growth procedure used here; clearances outside this range result in melt wipe-off problems.

All reagents and chemicals used in these experiments were of the highest purity obtainable (electronic grade when available).

GaAs used for the source wafer and growth melt solute was NRL undoped high purity material discussed elsewhere in this report. Prior to use, the GaAs was cleaned in HCl and in a solution of bromine and methanol. Tin used for doping was "six nines" grade from United Mineral & Chemical Co.

GaAs semi-insulating substrate material was grown at NRL. Preparative and growth procedures for this material are described elsewhere in this report.

Water vapor content of the effluent hydrogen stream from the reactor was measured with a Panametrics Model 2000 Hygrometer and normally ranged between 0.1-0.3 ppm during growth experiments.

Substrate Preparation

Boules of GaAs were prepared by the PBN-LEC process described elsewhere in this report and cut into slices with an annular saw. Two orientations were used: 3^{o} off the (100) toward the (110) and exactly ($\pm$ 0.5^{o}) on the (100). After scribing and cleaving to size (1 x 1 cm) the substrates were chem-mechanically polished with a solution of bromine in methanol on a rotating PAN-W pad. The substrates were cleaned ultrasonically in trichloroethylene (TCE), acetone, methanol and 2-propanol.

Immediately prior to insertion in the epitaxial reactor the substrate was cleaned by a procedure similar to that of Morkos and Eastman:[19] ultrasonic

cleaning in TCE, hot TCE, acetone, methanol, hot methanol, water and 2-propanol followed by etching for 4 min in a freshly prepared 511 solution (5 vols. conc. H_2SO_4 added drop wise to a cooled solution of 1:1 H_2O and 30% H_2O_2). The substrate was placed under water for 20 min then an equal volume of HCl was added. After 5 min the substrate was rinsed quickly in water then blown dry with high purity argon and inserted in the reactor.

Growth Experiments

Growth Procedure. - Growth melts were prepared from gallium, gallium arsenide and tin (as required); the quartz tube was purged overnight with palladium diffused hydrogen for safety and to reduce water vapor in the effluent gas stream to minimum values (ca 0.1 ppm). Melts were baked out above their saturation temperature (ca. 739°C) for 24 hrs after preparation. After the initial bakeout the melt was cooled, the furnace tube opened and a source wafer and prepared substrate inserted in the appropriate parts in the slider. After an overnight hydrogen purge the furnace was rolled on to the tube and the reactor was heated to ca. 738°C. After 30 min the source wafer is slid under the growth melt to begin melt saturation. After 1 hr of saturation, and with melt and source wafer still in contact, 0.3°C/mm ramp cooling is begun. Typically, the melt is equilibrium cooled for 3°C to establish a uniform temperature ramp. The substrate is then slid under the Ga etch solution for 15 sec. and is then, with continued cooling, slid under the growth melt. Cooling is continued until a layer of the desired thickness is grown. Typically, 40 sec. growth gives a layer 3000Å thick, as determined by C-V measurements. When growth is completed, the substrate is slid from under the growth melt and the furnace rolled off to cool the melt and grown layer.

In an alternate growth procedure the source wafer is removed from the growth melt before cooling is begun; under these conditions supersaturation

of the melt is produced. After cooling for, typically, $3^{o}C$, the epi layer is grown as described above while ramp cooling continues. This supercooling regime provides a driving force for wide spread nucleation of layer growth. Such driving force may be necessary or desirable if the substrate surface does not wet uniformly under equilibrium cooling conditions because of the presence of oxide or other impurities. The thickness of thin layers may be more difficult to control under the supercooling regime and the doping of the laeyr may be less uniform because of the non-equilibrium growth conditions. While the supercooling regime can be used with a pregrowth gallium etch, we find the etch eliminates the need for supercooling: the freshly etched surface allows uniform nucleation under equilibrium cooling. Carrier concentration profiles, as determined by C-V plot (Fig. 16), indicate uniform tin doping. A full discussion of cooling and epi growth regimes is found in reference 20.

Characterization of Layers

Grown layers are cleaned with 1+1 HCl to remove any drops of gallium adhering to the edges (a small drop on the trailing edge of the wafer is common) and examined by interference contrast (Nomarski) microscopy. Other characterization methods have included Van der Pauw and C-V measurement, and fabrication of devices upon the layer. FET structures and characterizations have been made in house and by outside laboratories. The results of these studies are reported separately.

Discussion

Gallium Etch of Substrate

The gallium etch of the substrate should remove the thermally damaged and/or converted layer and leave a surface usable for layer growth. While an etch time as short as 1 sec. has been shown to remove the conversion layer

from chromium doped semi-insulating substrates, the surface after such a brief etch (achieved by rapid passage under the gallium etch well) is covered with ridges running perpendicular to the direction of travel and spaced 20-50μ apart. Interference microscopy indicates the ridges to be 0.1-0.2μ high. These ridges are replicated in the grown layer and give a surface less than ideal for device fabrication. A gallium etch of 15 sec. results in a surface that is specular to the unaided eye and, under Nomarski microscopy, is uniform, slightly roughened and free from major features. Figure 17 illustrates such a surface. Epi layers grown after the 15 sec. etch are quite suitable for device fabrication.

During the 15 sec. gallium etch it appears that between 50-100μ of material are dissolved; literature values[24] are consistent with our own estimates. Repeated use of the gallium etch solution results in a less uniformly etched substrate and it appears that the GaAs content of the etch solution is a small though significant variable in the functioning of the etch process. Normally between 6 and 10 acceptable layers can be obtained before replacement of the gallium etch solution becomes desirable.

Bake out of Melt

Bake out times of the growth melt after loading a prepared substrate have varied upwards from 1 hr. A long bake out offers the advantage, in principle, of minimizing volatile impurities in the melt (e.g. oxygen) but presents increased problems with conversion and degradation of the substrate surface. A thermally damaged area of a substrate surface after 20 hrs heating at 735°C is shown in Fig. 18. The substrates were protected under the end of the graphite reactor; the features shown (ca. 10 x 40μm) developed along the substrate edge nearest the flowing hydrogen stream. Examination by scanning electron microscope and electron probe show that these areas are gallium rich indicating that arsenic loss may play a major role in the thermal degradation of the substrate surface.

We have chosen a 1.5 hr bake out time at a temperature ca. 3°C above the growth temperature of 735°C to balance thermal degradation and impurity bake out; the best substrates do not convert under these conditions and the melt is not saturated. Nomarski microscopic examination of a surface heated 1.5 hrs shows only a very slight uniform roughening.

A cooling ramp of 0.3°C/min was normally used; a small (1-2 mm) drop of gallium frequently remains on the trailing edge of the wafer after layer growth. Layer growth under standard conditions (15 sec. gallium etch + 40 sec. growth) but with steeper cooling ramps (ca. 2°C/min) have resulted in large amounts of gallium being left on the surface of the wafer; up to 1/3 the surface may be covered. These results suggest that cooling rate and/or temperature gradients within the melt affect wipe off of the melt and thereby may determine, at least in part, the amount of gallium retained on the surface.

Cusp Formation

Cusps are pointed or slightly rounded projections or depressions in the surface of the epi layer. While cusps are not normally associated with large areas of ungrown substrate they usually do represent small discontinuities in the layer surface and may interfere with device fabrication and/or performance.

Cusps have been attributed to GaAs crystallites in the melt,[21] to melt/substrate wetting problems and to growth rate.[19] To investigate the mechanism of cusp formation we have conducted growth experiments at short growth times. Fig. 19 shows typical partial layer growth after 20 sec. growth at 735°C following 1°C equilibrium cooling (at 0.3°c/min) and a 15 sec. Ga etch on a substrate oriented 3° off the (100) toward the (110). Figure 20 shows growth after 40 sec. under similar conditions. Cusp densities of typical best growth on these slightly off oriented substrates were mid $10^3/cm^2$. The inclined flat surfaces of the growth islands in Fig. 19 suggest that misorientation may influence

growth: the cusps and unevenness in Fig. 20 could have resulted from incomplete and imperfect joining of the growth islands in Fig. 19. Epi layer growth on substrates oriented exactly on the (100) was flat, with significantly lower cusp densities (mid to upper 10^2/cm).

The layers of Figs. 19 and 20 were grown after only 1^o equilibrium cooling. Under these conditions the cooling ramp may not be uniformly established. Forty seconds growth on perfectly oriented substrates after 3^o equilibrium cooling gave flat, low cusp density layers e.g. Fig. 21; while it may not be practical to separate completely cooling ramp and orientation effects it is possible that both variables affect layer surface quality through cusp formation.

Still another possible cause of cusp formation may be seen in Fig. 22 which shows a gallium etched substrate surface (oriented 3^o off the 100 toward the 110). While most of the gallium etched substrate surface is as shown in Fig. 17, etch features shown in Fig. 22 are present in many cases. The etch features in Fig. 22 correspond in size (5-20μ), shape (roughly circular), frequency (10^2-10^4/cm^2) and distribution (more numerous near the substrate edges) to cusps on grown layers and a relationship between the two appears probable. The cause of the etch features is not definitely known but they are apparently the result of differential dissolution of the substrate, inclusions and/or crystalline imperfections. The etch features are much less common on substrates oriented exactly on the (100); substrate orientation may therefore also be significant.

Tin Doping and the Effective Distribution Coefficient

Growth melts were doped with approximately 3 mole percent tin. From C-V measurements of carrier concentrations or layers grown from two separate melts it is possible to calculate effective distribution coefficients, k, for tin under the growth conditions described above. These distribution

coefficients together with literature values are summarized in Table I. NRL layers which were grown on substrates exactly on the (100) and 3° off it toward the (110) showed no significant difference in k.

TABLE I

Distribution Coefficients for Sn in GaAs LPE

	distribution coefficient, k	remarks
Melt 12-14N	9.0×10^{-5}	This work, T=735°C
Melt 12-71N	8.9×10^{-5}	" " "
Rosztoczy	7.9×10^{-5}	Ref. 22, T=725°C
Migitaka	8.2×10^{-5}	Ref. 23 T=730°C

Device Characterization of Epitaxial Layers

A detailed description of electrical characterization of epi-layers is the subject of a separate report;[25] what is presented here is a summary relating primarily to epi layer growth.

Although a variety of ways exist to electrically characterize an epitaxial layer the usual definitive method is to make the desired device (here, the FET) upon it and evaluate device performance. Within a given fabrication technology, differences in device performance may reflect variations in material quality.

Devices were made on NRL epitaxial material at NRL and by an outside laboratory. While the results obtained to date are both preliminary and fragmentary they are also encouraging. Results obtained on NRL fabricated devices (on NRL LPE material grown by the Ga etch procedure) are summarized in Table II.

TABLE II

NRL FET Characteristics

Sample	Gate length, (microns)	Min. noise fig @ 8 GHz (dB)	Associated gain 8 GHz (dB)
NRL 12-29N(LPE)	1.5	5.4	8
NRL 12-78N(LPE)	1.5	5.1	4

The relatively high noise figures may be attributable to processing and/or design variables and may not truly reflect the properties of the material. A detailed discussion of the NRL device fabrication program can be found in reference 25.

Somewhat more encouraging results have been obtained on devices fabricated on NRL LPE material by an industrial laboratory. These results, with comparative data on other material are presented in Table III.

TABLE III

Comparative FET Characteristics

Sample	Gate length	10 GHz	
	Micron	noise dB	gain dB
NRL (12-43N)LPE, Industrial Lab fabrication	0.5	3.0	10.4
Industrial Lab LPE and fabrication (no buffer)	0.5	3.0	10.0
Industrial Lab VPE and fabrication (no buffer)	0.5	2.9	9.1
Industrial Lab, ion implanted	0.5	3.1	7.3

From the results in Table III, it appears that NRL LPE material grown with the etch back process but without a buffer layer results in devices slightly better than those obtained using non-etch growth processes. For equivalent noise figures at 10 GHz, higher gains are obtained on the NRL-LPE material than on either VPE or LPE materials. The device design used

in these evaluations was intended to maximize gain even at the cost of higher noise. Within the technology represented by the industrial laboratory, it appears that the NRL-LPE material offers a small but real advantage over other material. It should also be noted that the NRL-LPE material here is non-selected, unoptimized material, both with respect to substrate and epi growth; as the preparation/characterization feedback improves, considerable improvement in material quality is to be expected. The data now available indicate NRL-LPE material to be up to state-of-the-art standards.

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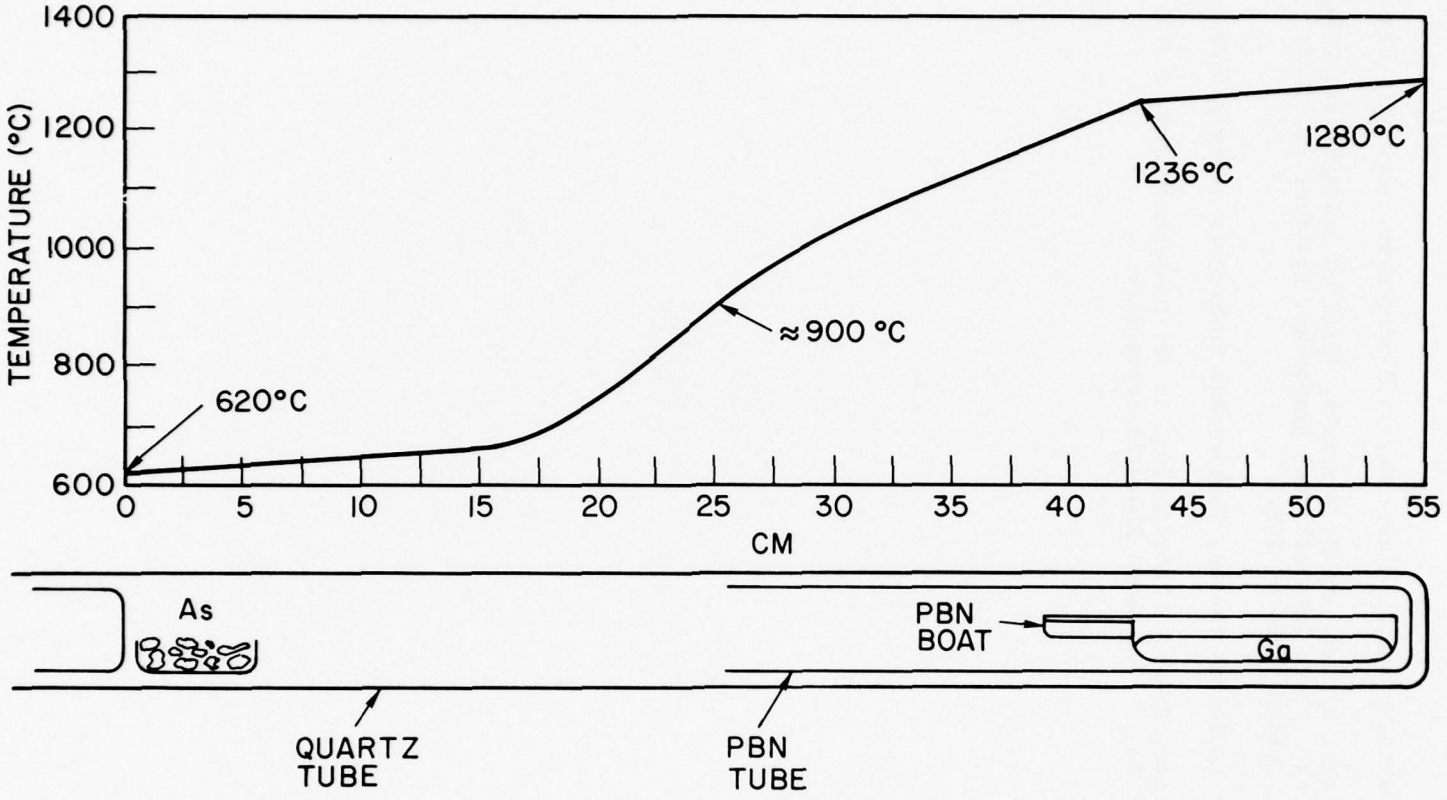

Fig. 1 — Gradient freeze apparatus

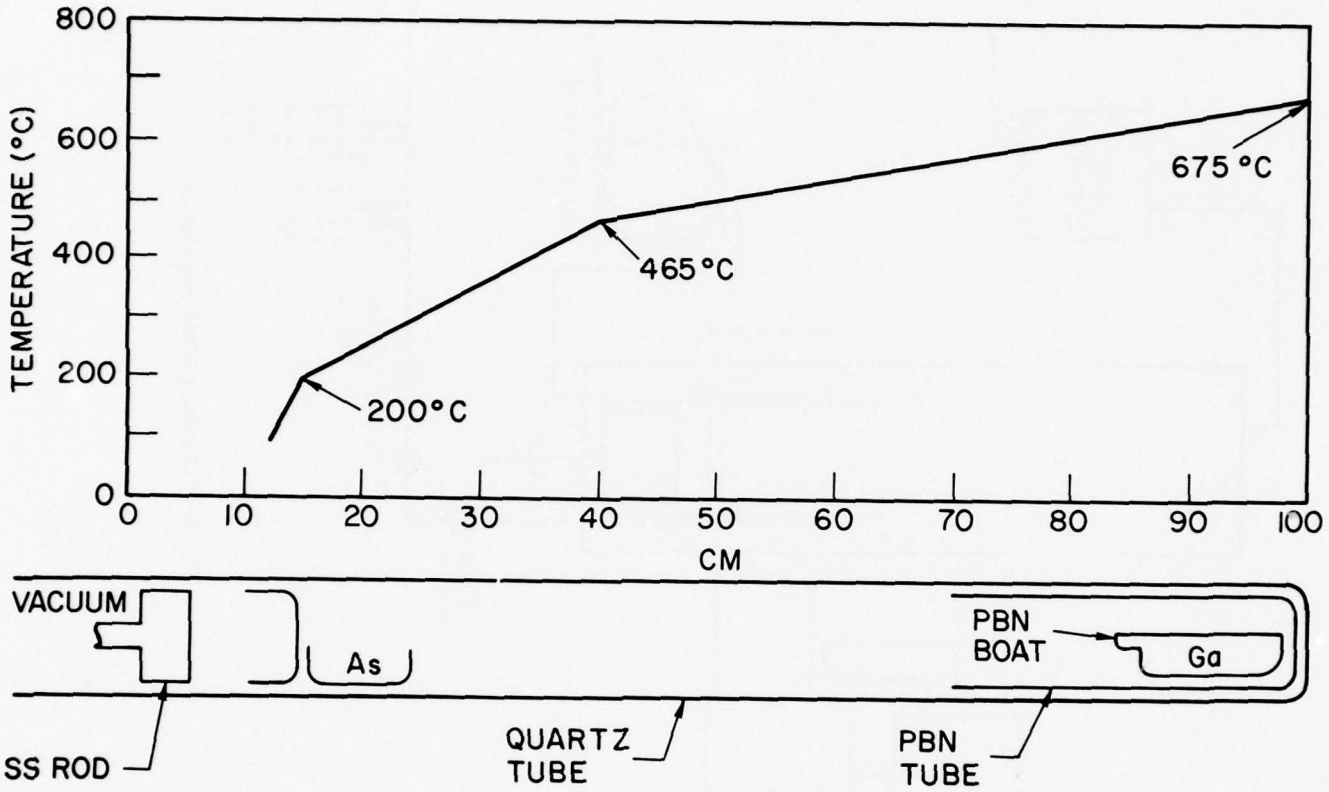

Fig. 2 — Vacuum baking arrangement

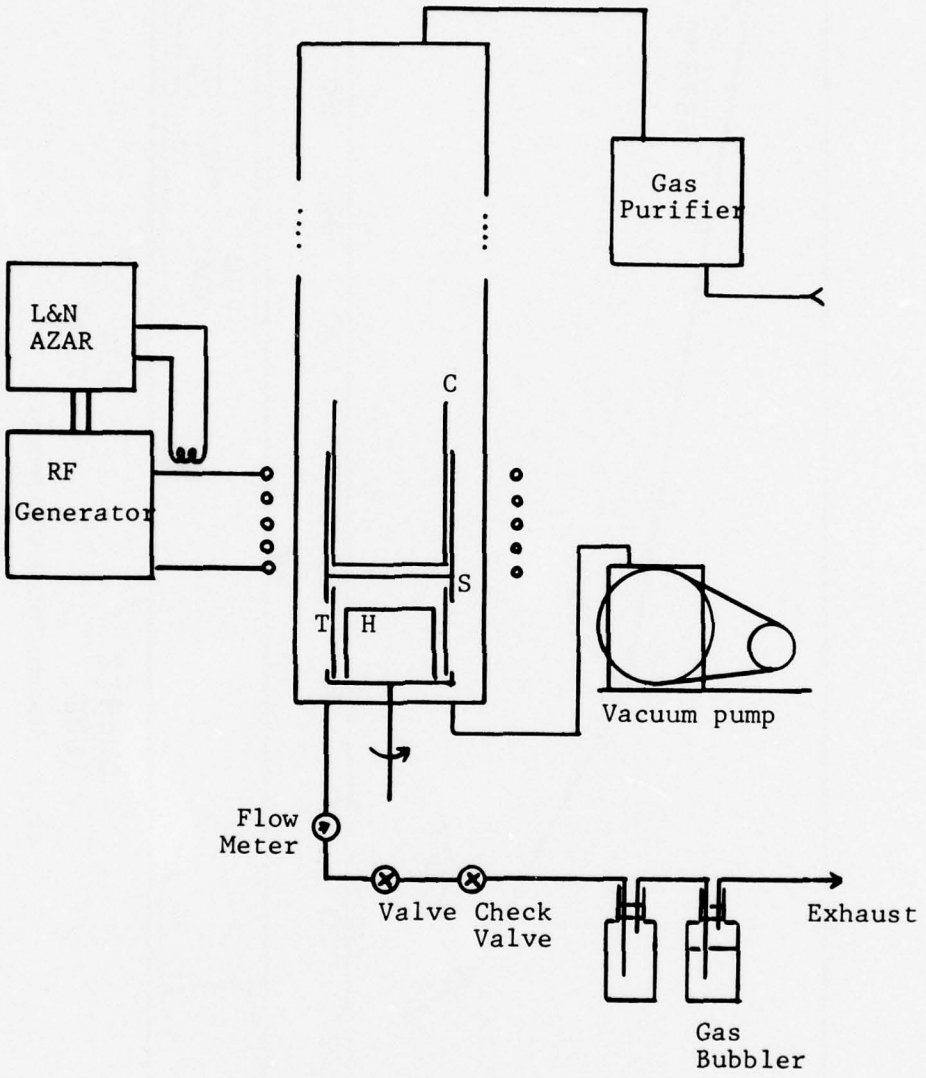

Fig. 3 — Crystal pulling apparatus

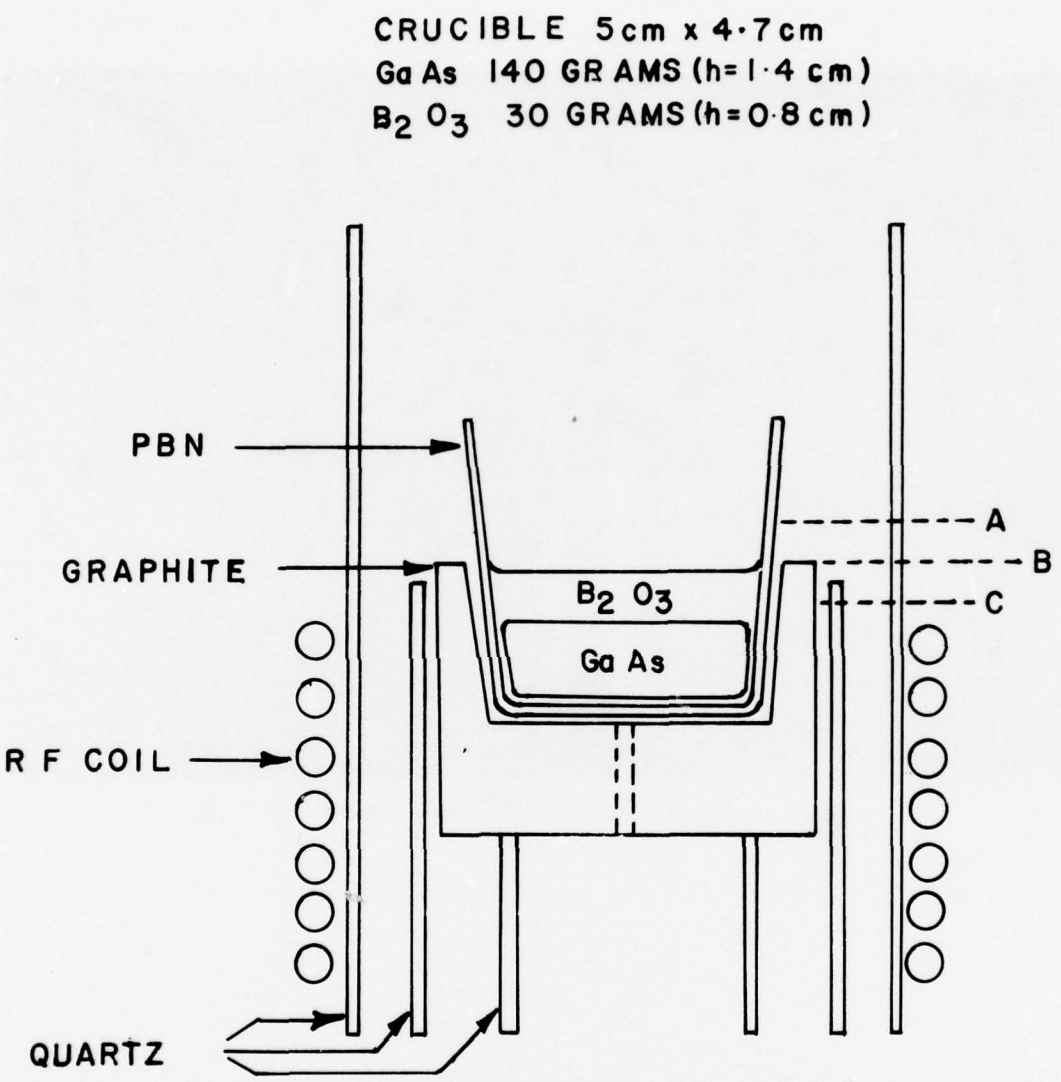

Fig. 4 — GaAs LEC crystal growth arrangement (to scale)

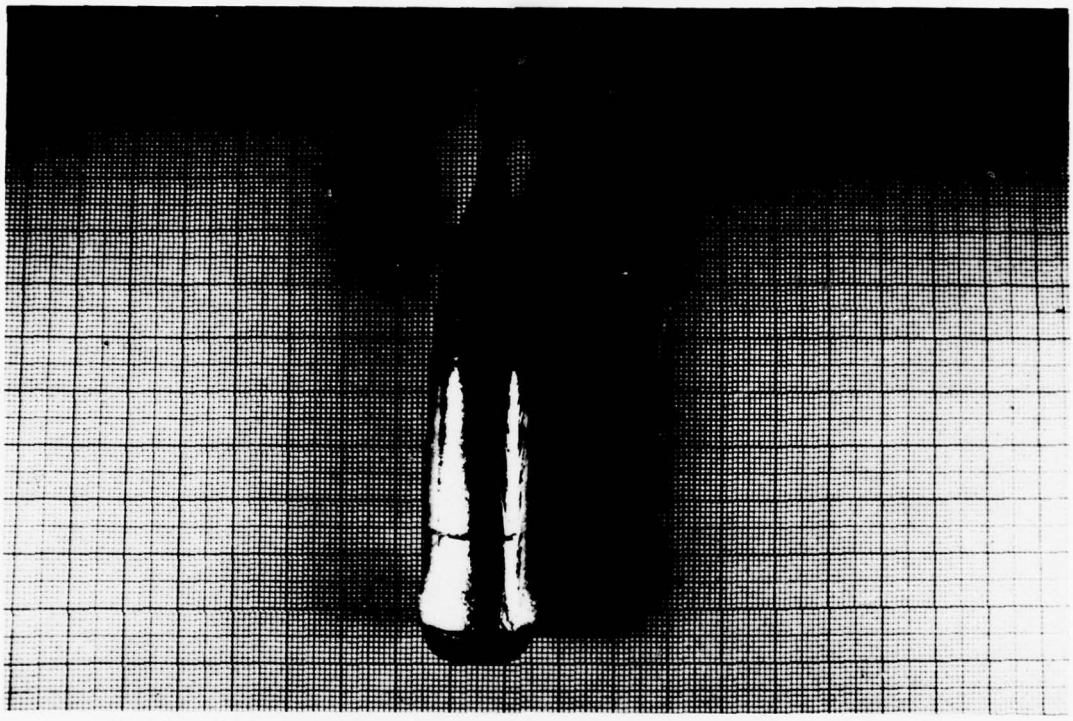

Fig. 5 — Typical LEC GaAs crystal

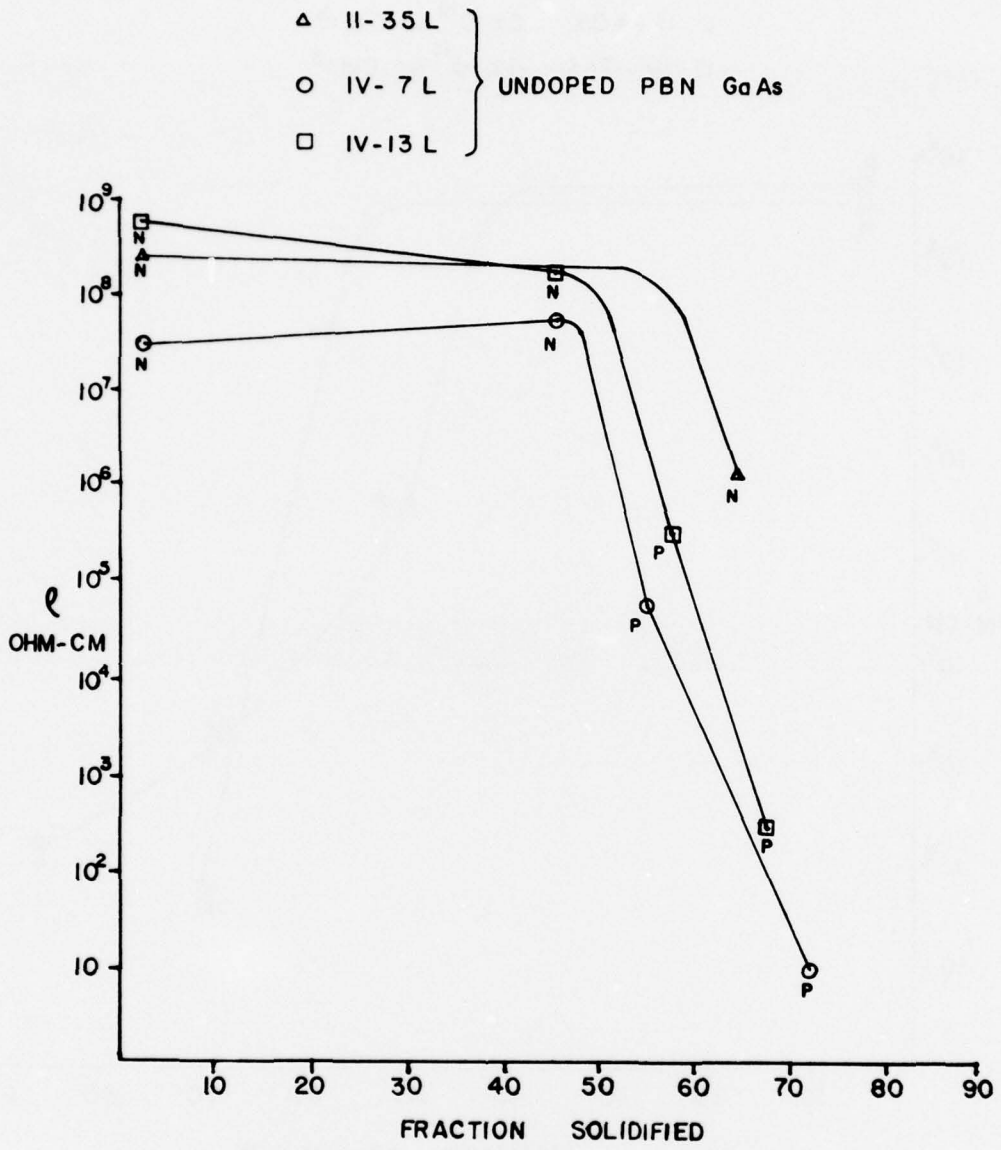

Fig. 6 — Electrical properties of undoped PBN-LEC GaAs crystal

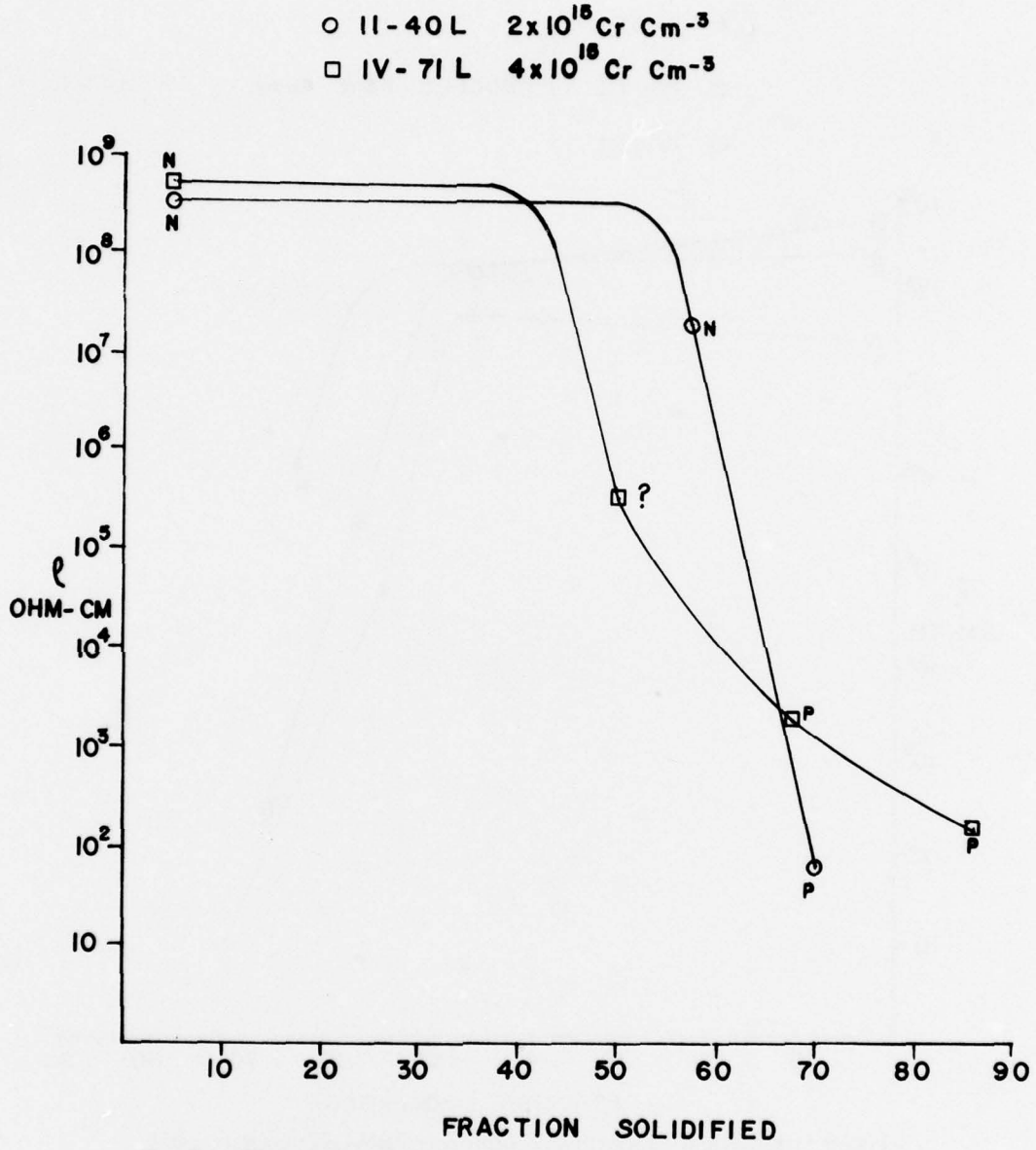

Fig. 7 — Electrical properties of Cr doped PBN-LEC GaAs crystals

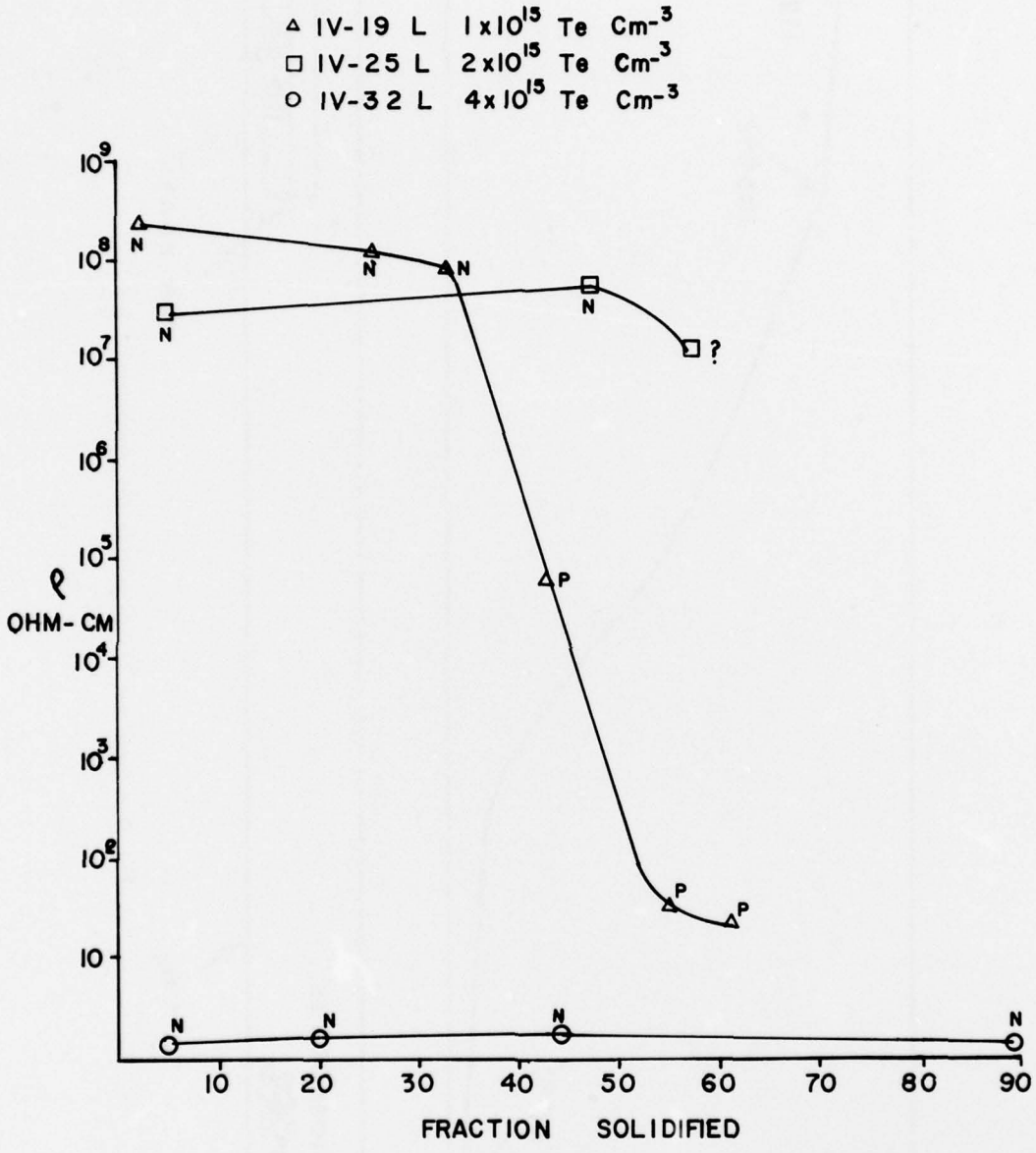

Fig. 8 — Electrical properties of Te doped PBN-LEC GaAs crystals

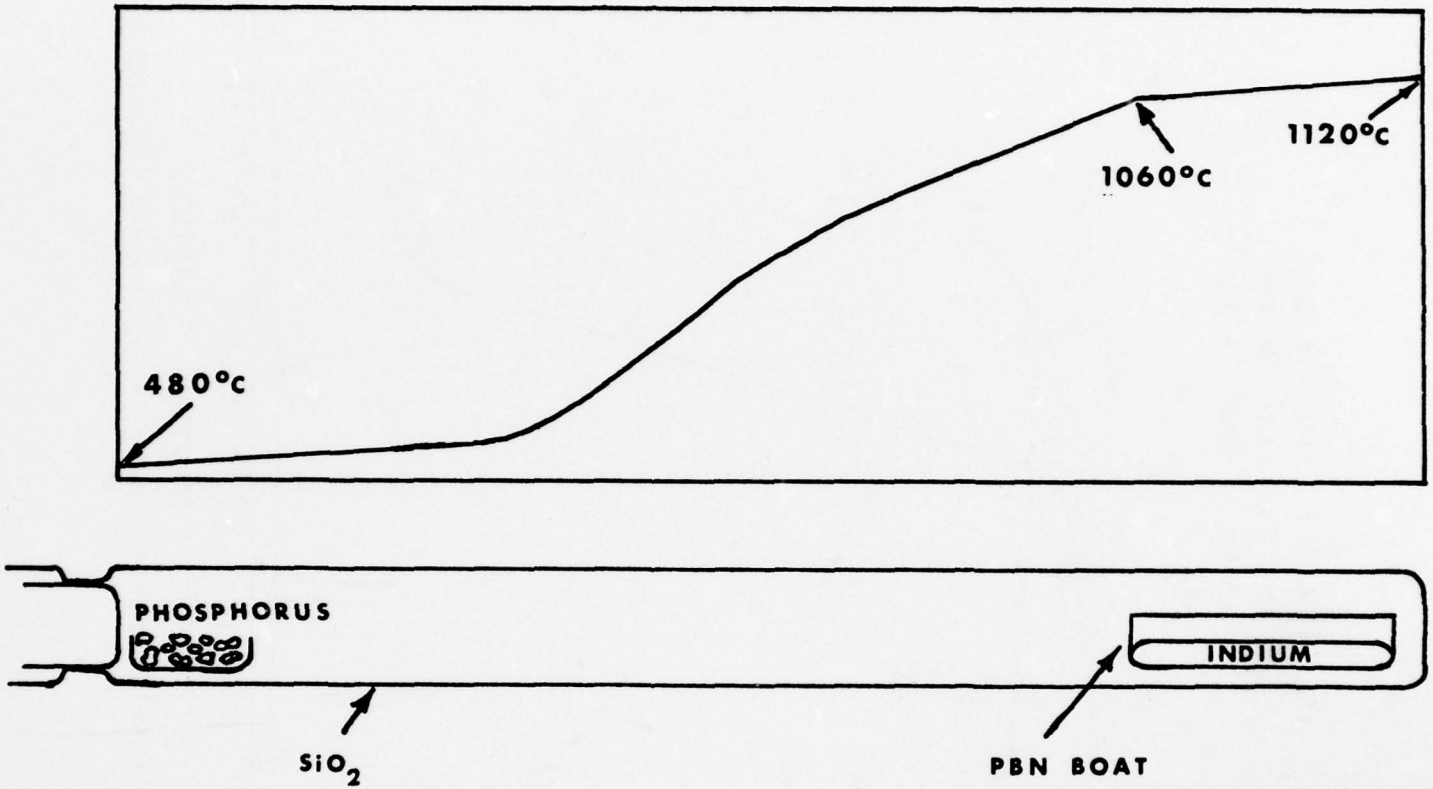

Fig. 9 — Gradient freeze profile for synthesis of InP

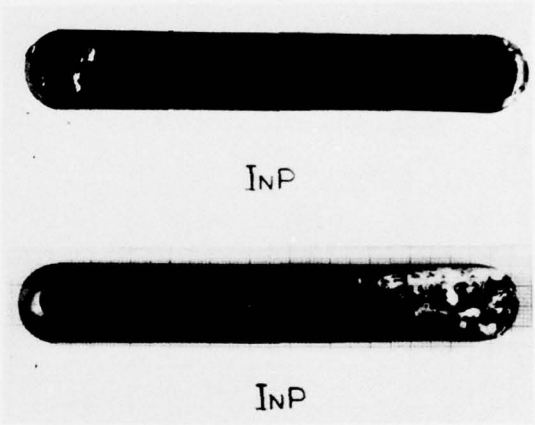

Fig. 10 — Compounded ingot of InP

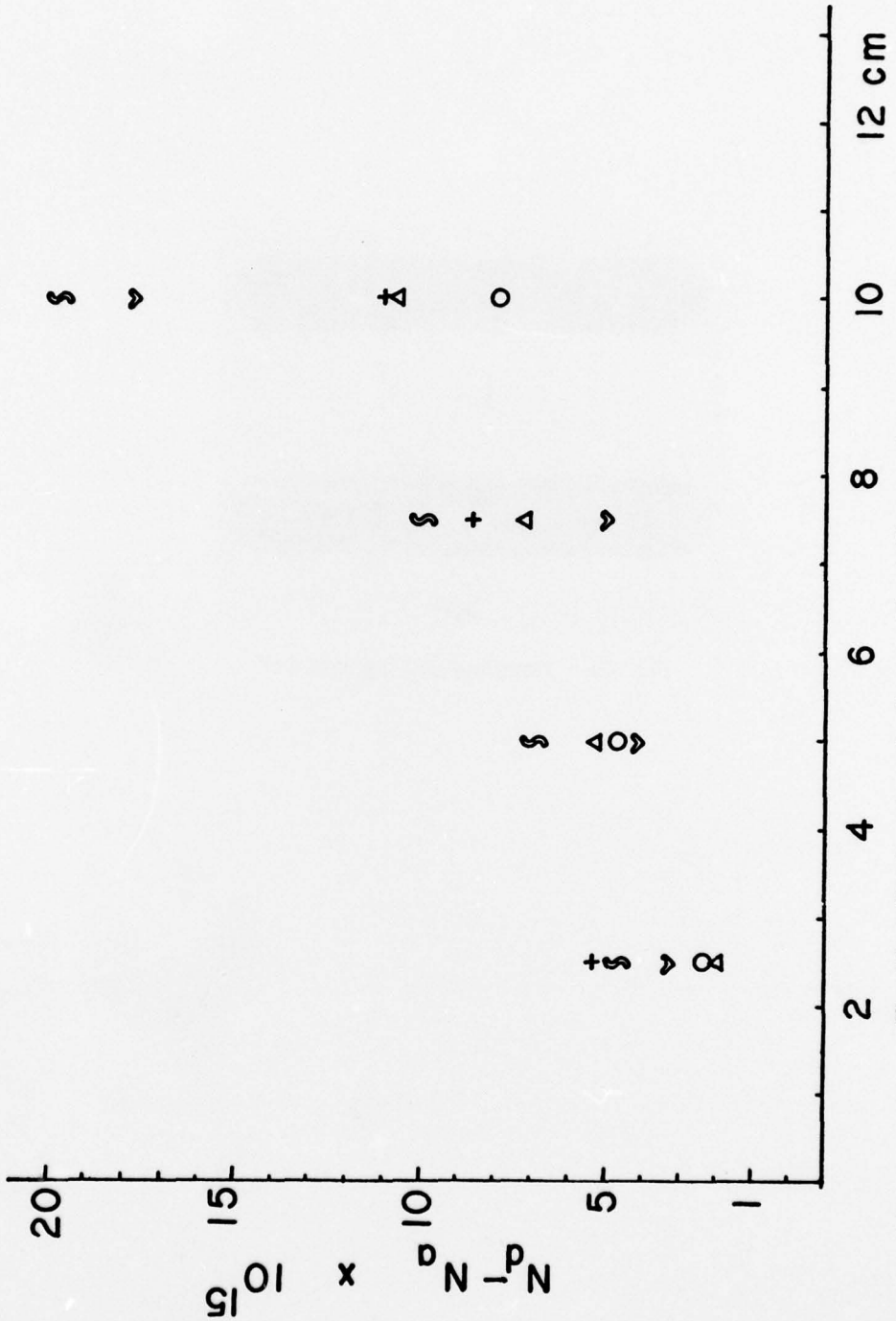

Fig. 11 — Carrier concentration profile vs distance for a series of InP ingots synthesized in PBN boats

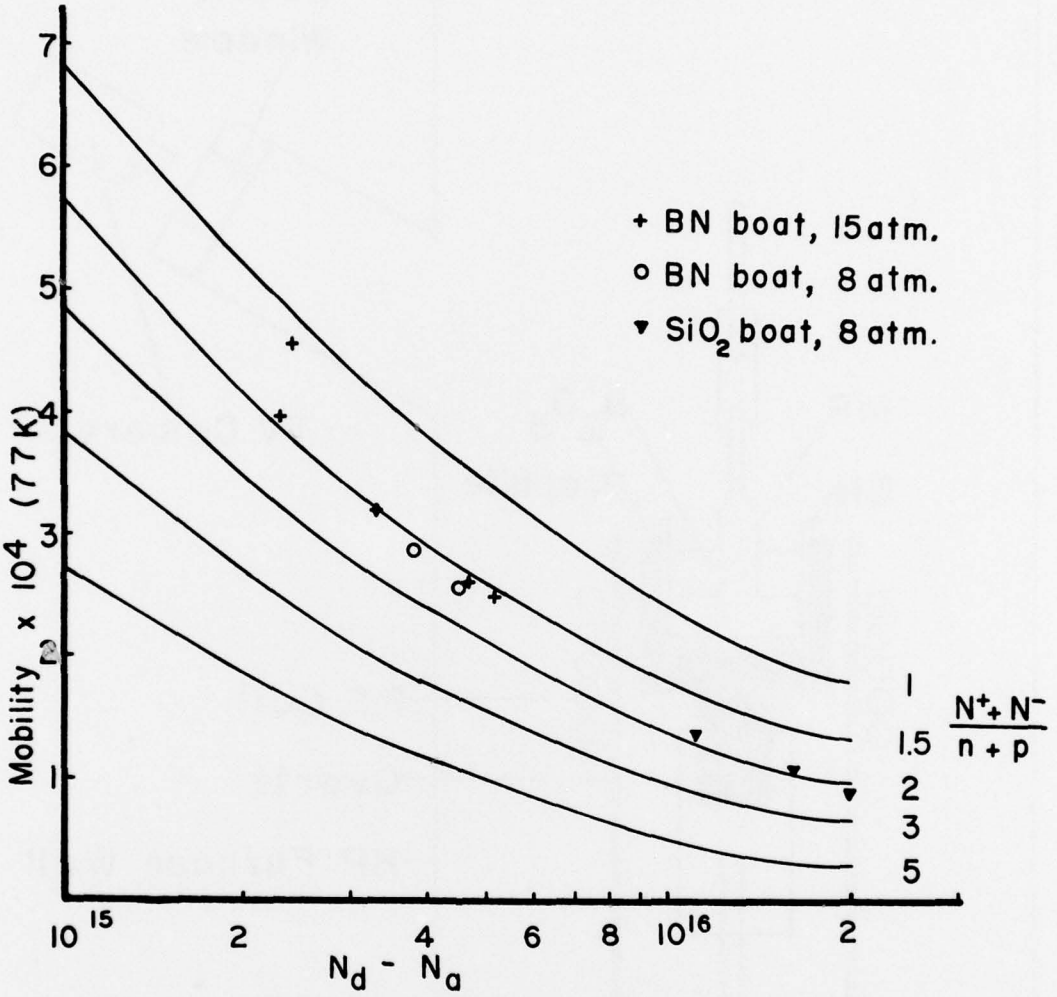

Fig. 12 — Hall mobility (77°K) vs carrier concentration for several compensation ratios

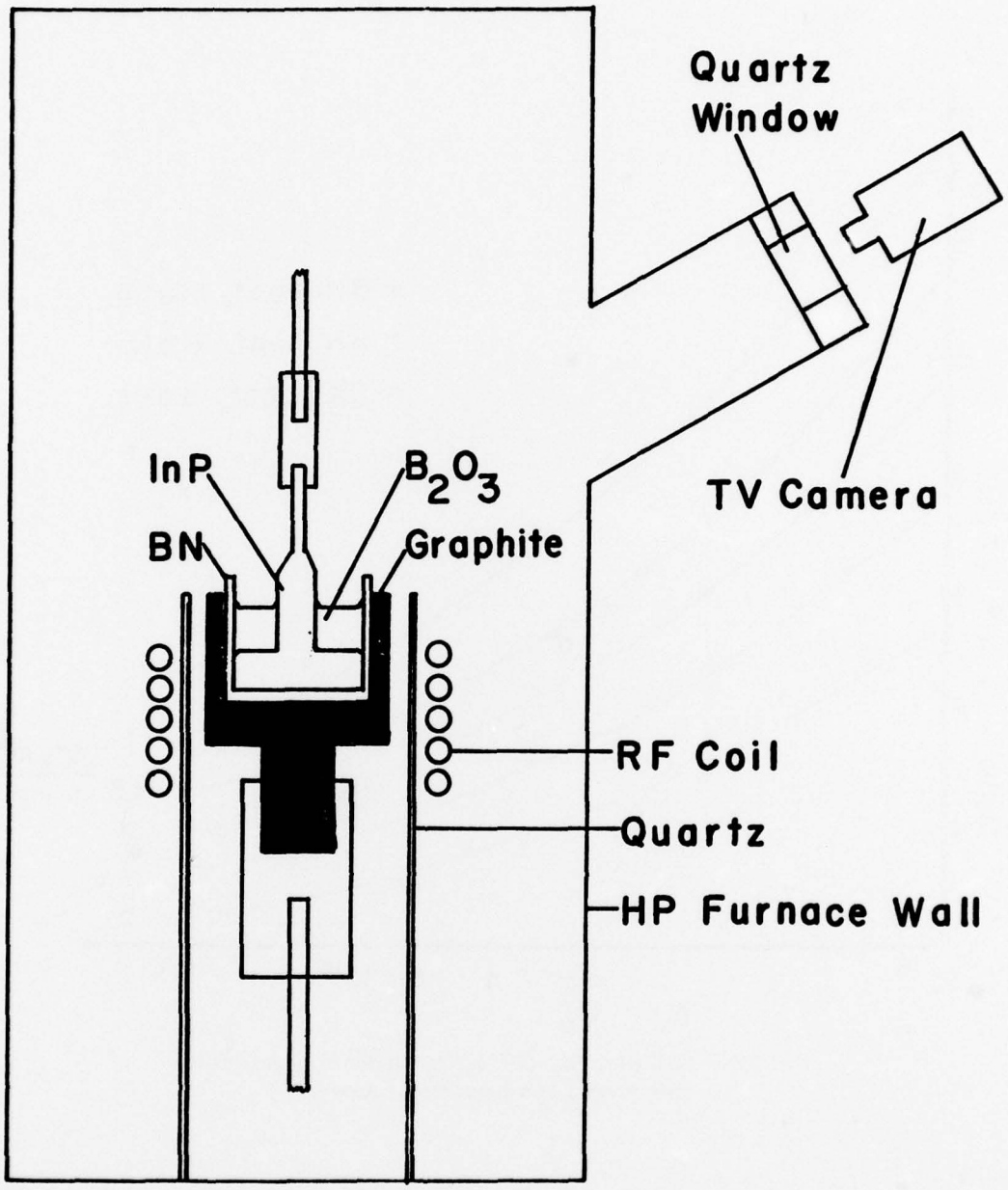

Fig. 13 — InP LEC crystal growth arrangement

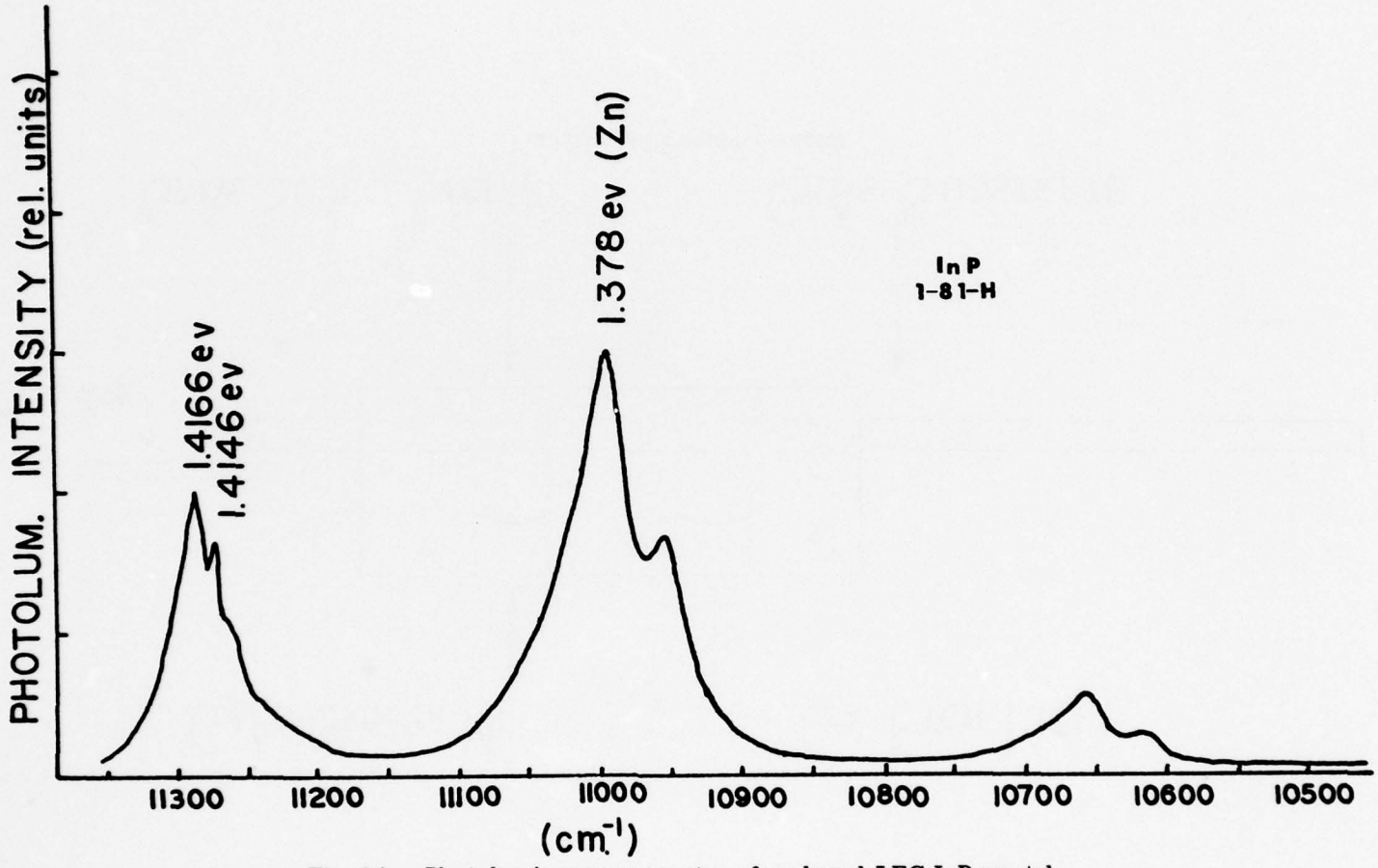

Fig. 14 — Photoluminescence spectra of undoped LEC InP crystal

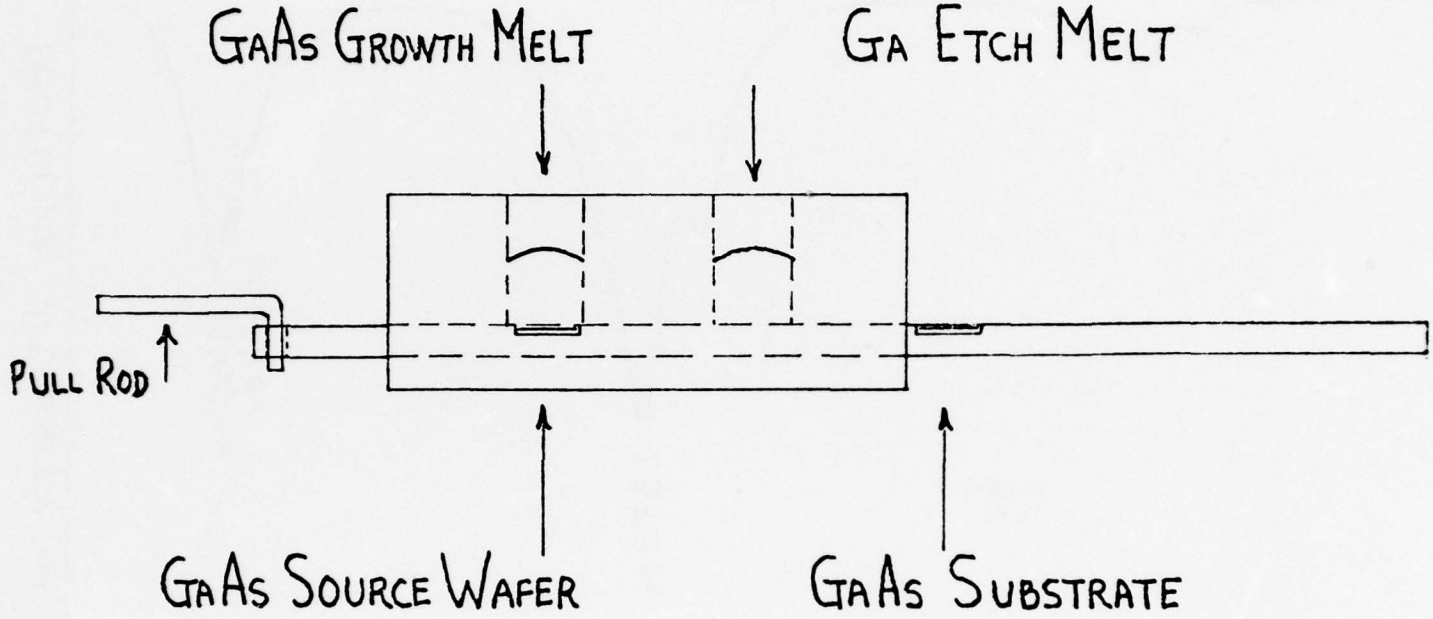

Fig. 15 — LPE growth reactor

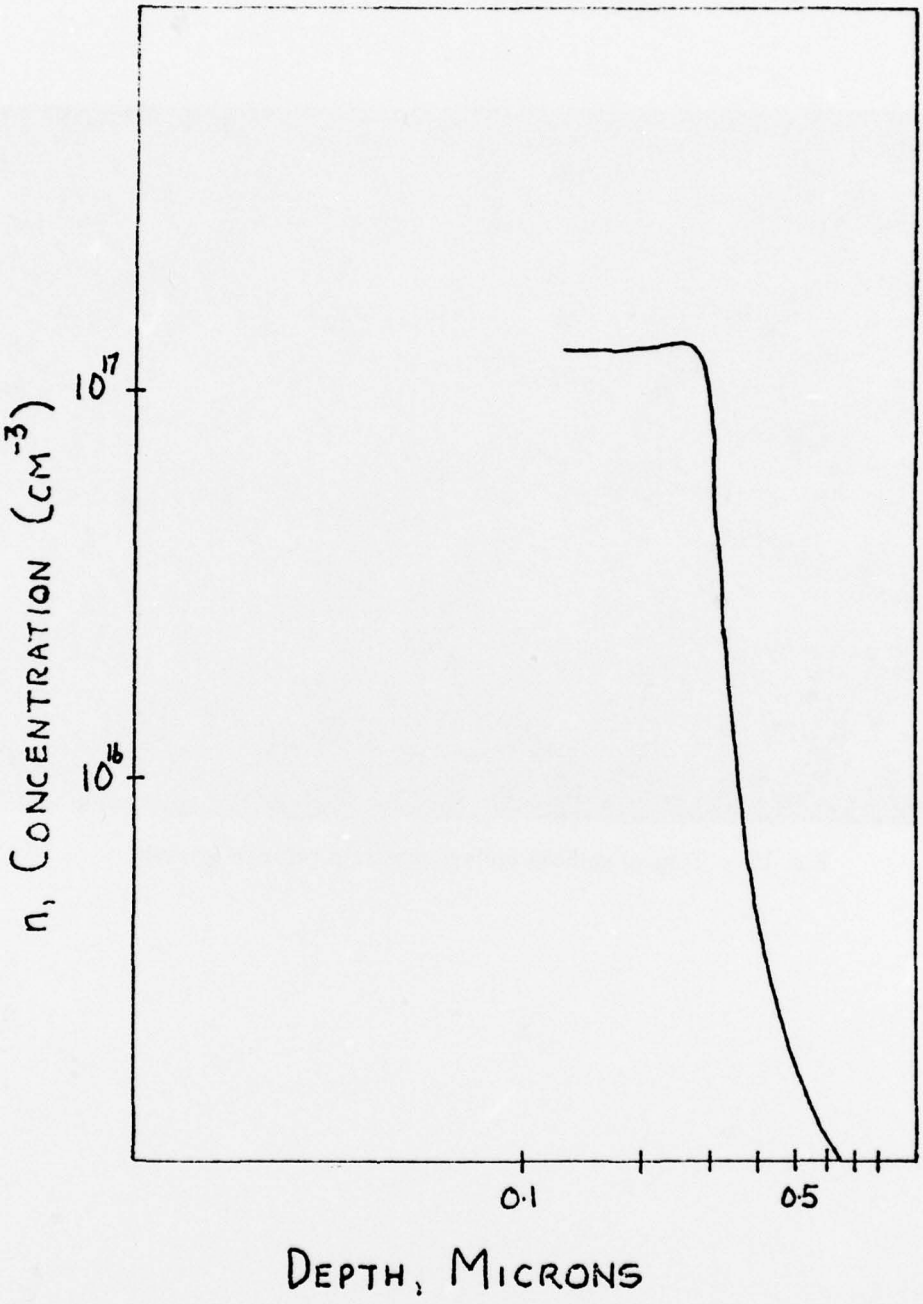

Fig. 16 — C-V doping profile

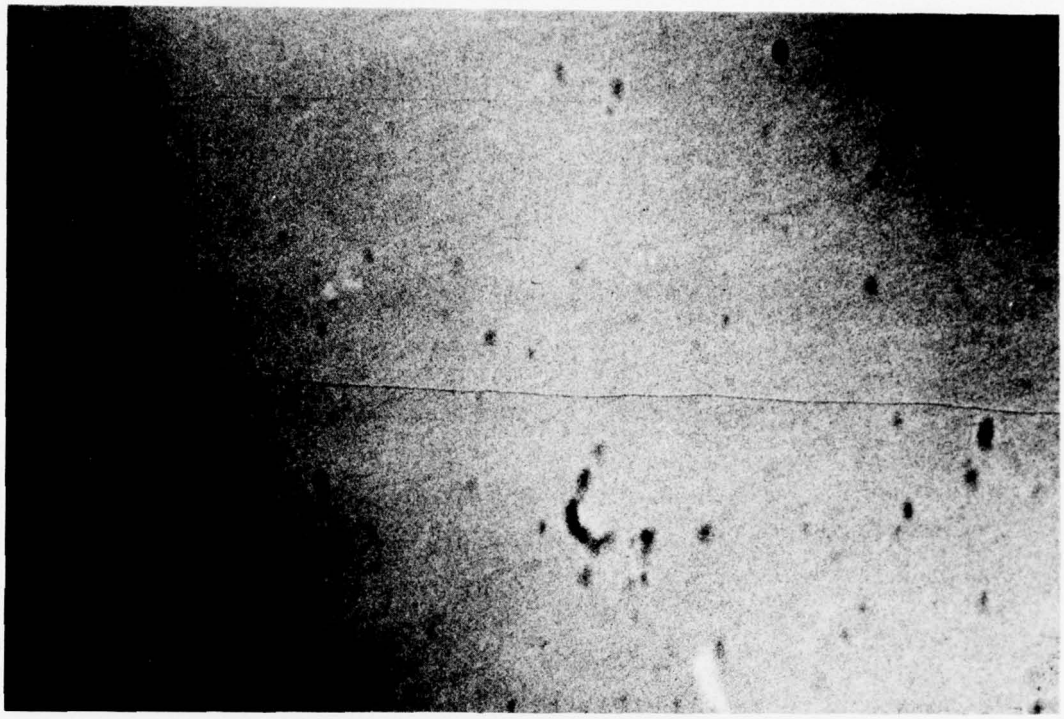

Fig. 17 — Typical gallium etched substrate prior to growth

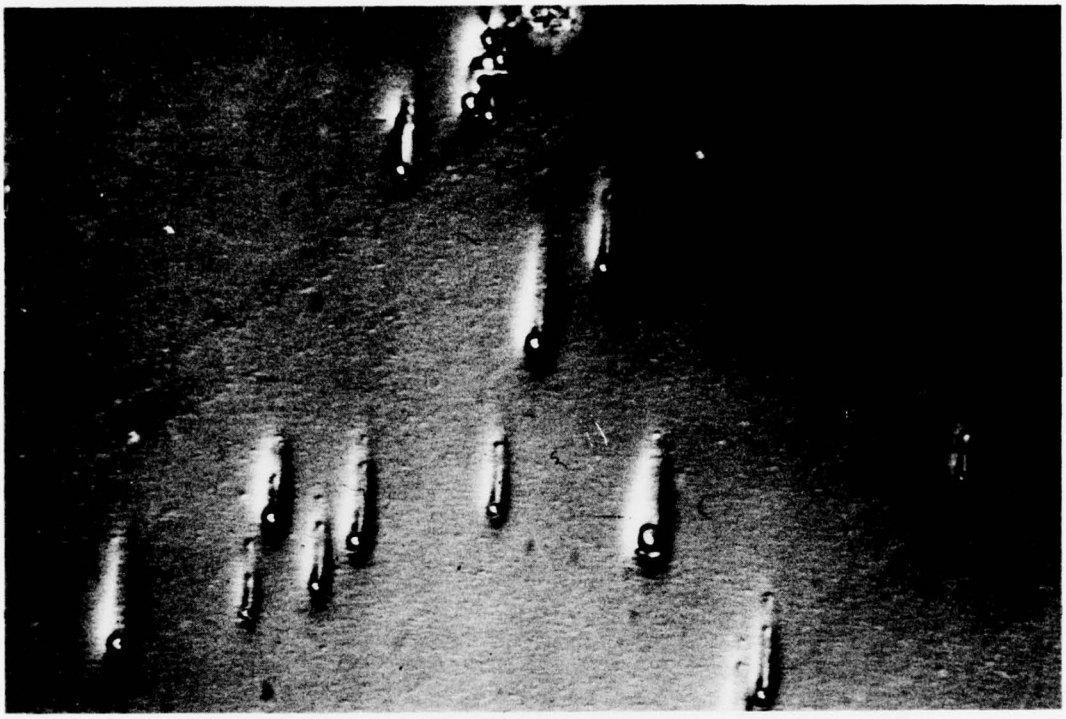

Fig. 18 — Thermally etched substrate, 20 hours - 735°C

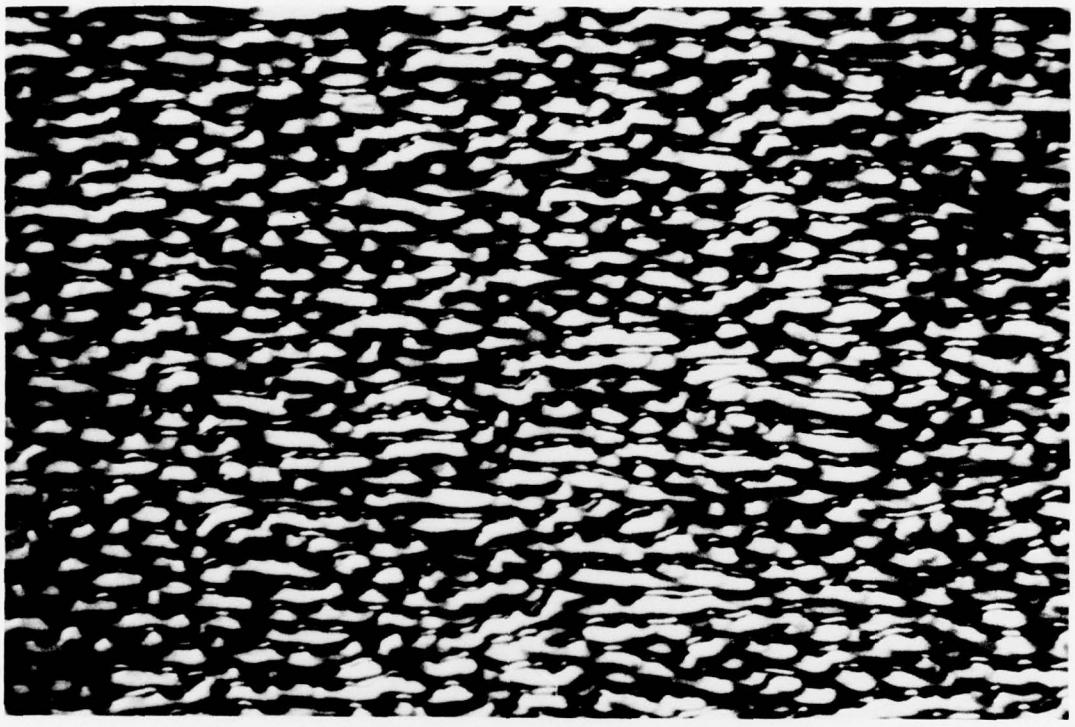

Fig. 19 — Typical partial layer growth, 20 sec - 735°C, equilibrium cooling

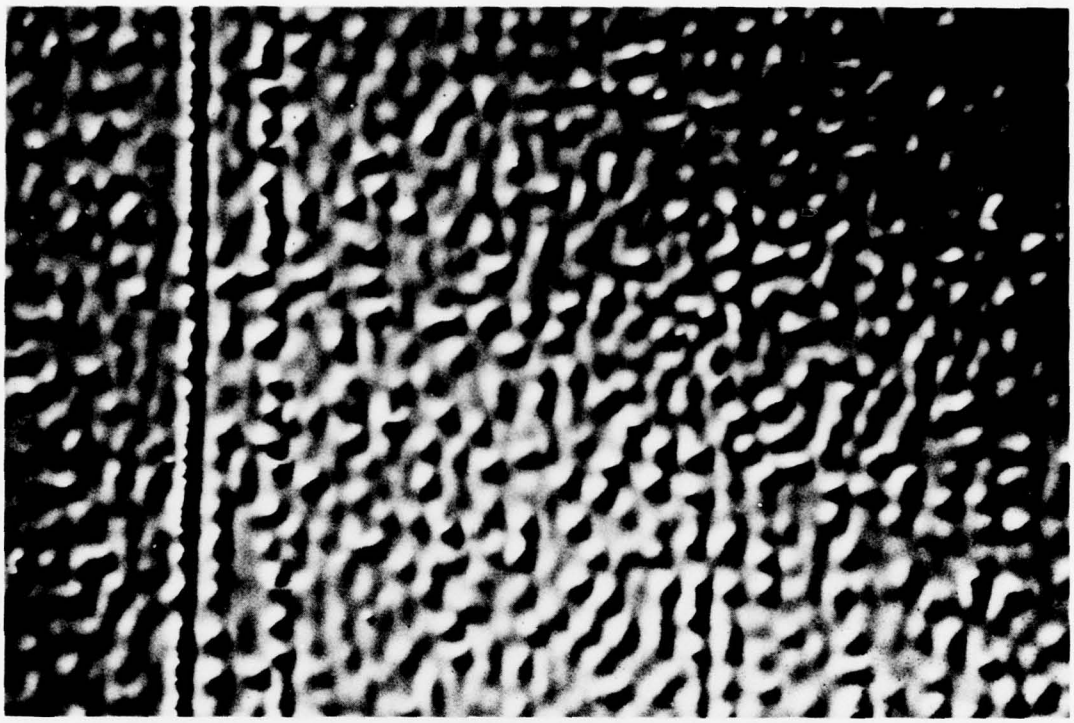

Fig. 20 — Typical layer growth, 40 sec - 735°C, equilibrium cooling

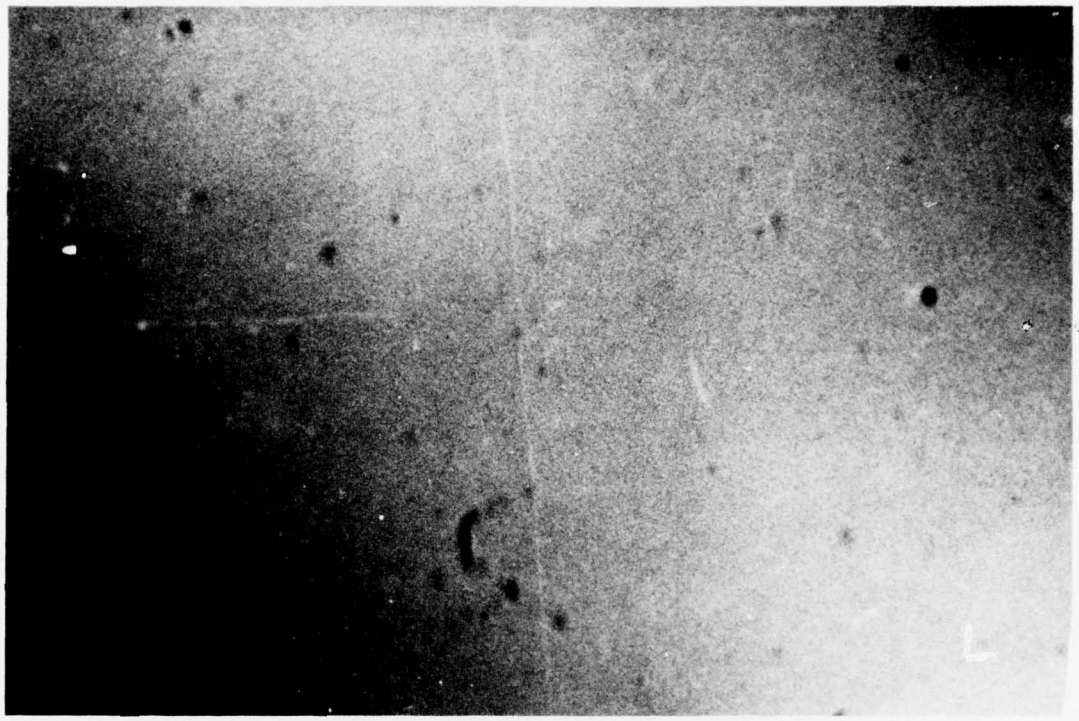

Fig. 21 — Layer growth on perfectly oriented (100) substrate

Fig. 22 — Gallium etched substrate surface oriented
3° off (100) → (110)